

Compal Confidential

Model Name : QILP2
File Name : LA-8262P

Compal Confidential

PT-Note Schematic Document

TBT SKU

2012-04-18

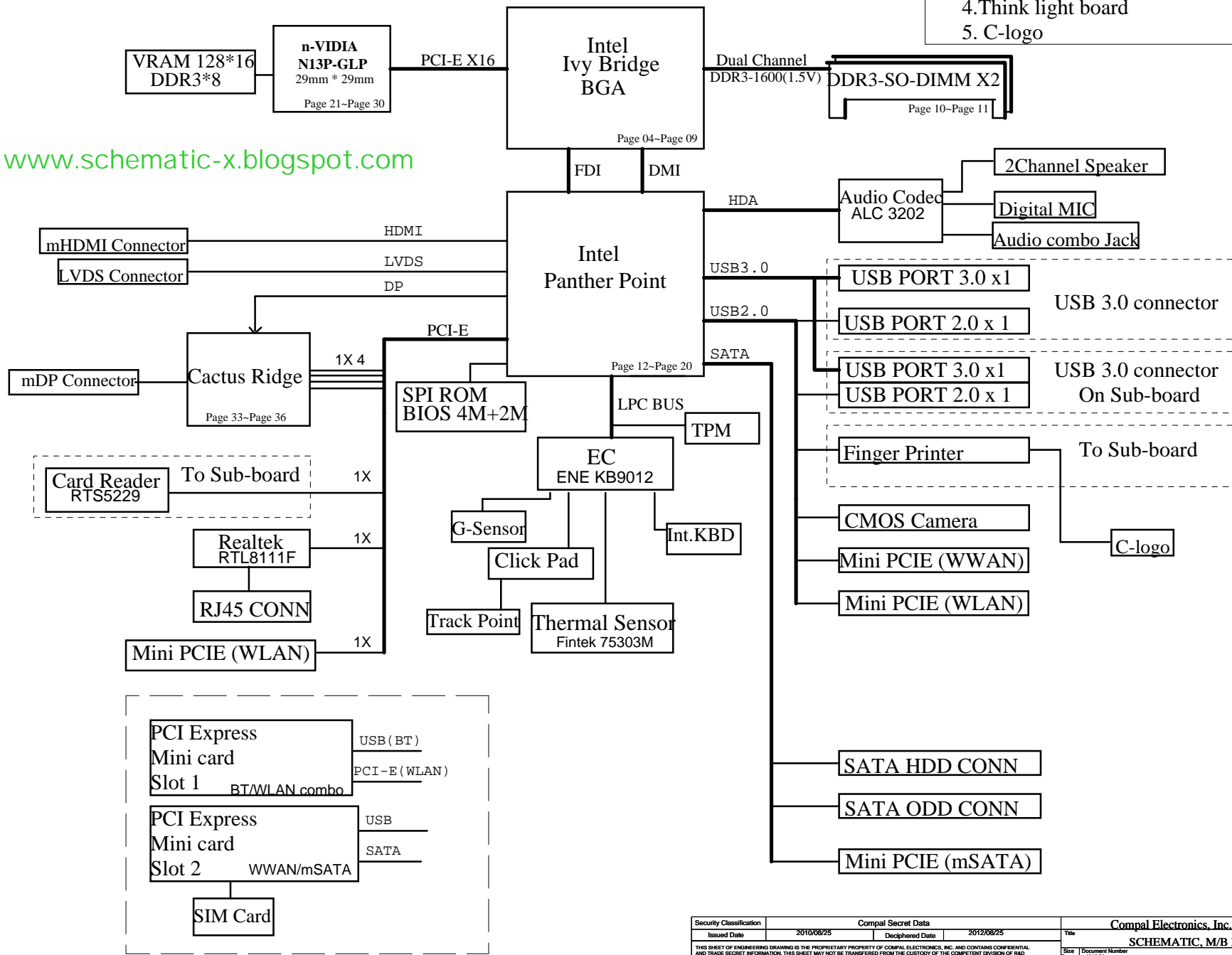
REV:1.0_0418B

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- Sub-board
- 1.Power on & DCIN Board
 - 2.Card Reader Board
 - 3.FP board
 - 4.Think light board
 - 5. C-logo

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Voltage Rails

Power plane	+B	+5VALW +3VALW	+1.5V	+3.3VM +1.05VM	+5VS +3VS +1.8VS +1.5VS +1.05VS +VGFX_CORE_AXE +CPU_CORE +VCCSA +0.75VS
					+3VS_VGA +1.05VS_VGA +1.5VS_VGA +VGA_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
M3	O	O	O	O	X
S4	O	O	O	X	X
S5 - AC	O	O	X	X	X
S5 - BATT ONLY	X	X	X	X	X
G3 - NO AC & BATT	X	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON		H	H	H	ON	ON	ON
S3 (Suspend to RAM)		L	H	H	ON	ON	OFF
S4 (Suspend to Disk)		L	L	H	ON	OFF	OFF
S5 (Soft OFF)		L	L	L	ON	OFF	OFF

BOM Structure @ : Un-pop.

UMA@ : UMA only
PX@ : Muxluss

ME@ : ME components
H2G@ :
S2G@ :

TPM@ : TPM Function.
BT@ : BT module.

ID4@ : LID S4 Function.
AOAC@ : AOACFunction.
sensor@ : sensor Function.

SBA@ : SBA Function.
NOSBA@ : NO SBA Function.

BOARD ID Table

Board ID	PCB Revision
0	N/A
1	0.2
2	0.3
3	
4	
5	
6	
7	

EC SM Bus1 address EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery		16H	EMC1403-2(DDR,WLAN)	1001-101xb	9AH
Smart Charger		12H	SB-TSI		96H
			GPU		9EH

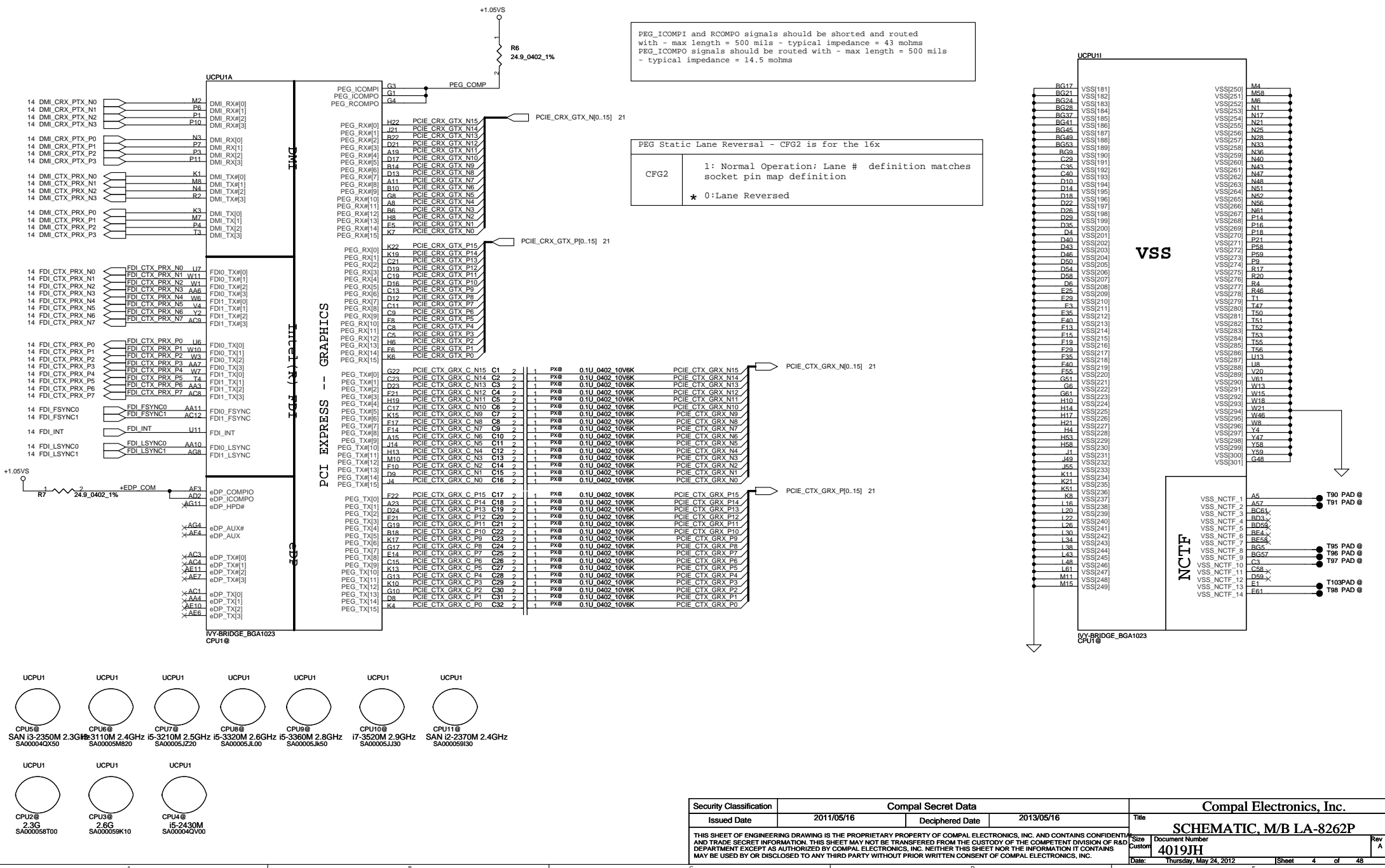
SM Bus Controller 0

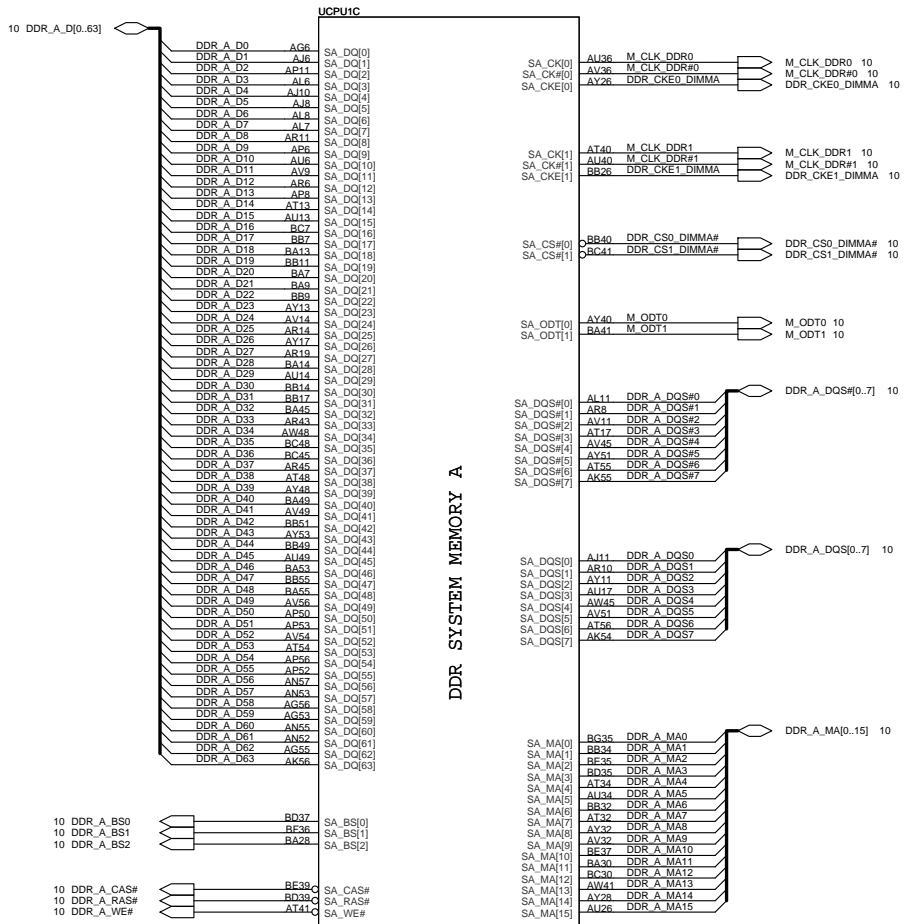
Device	Address	HEX
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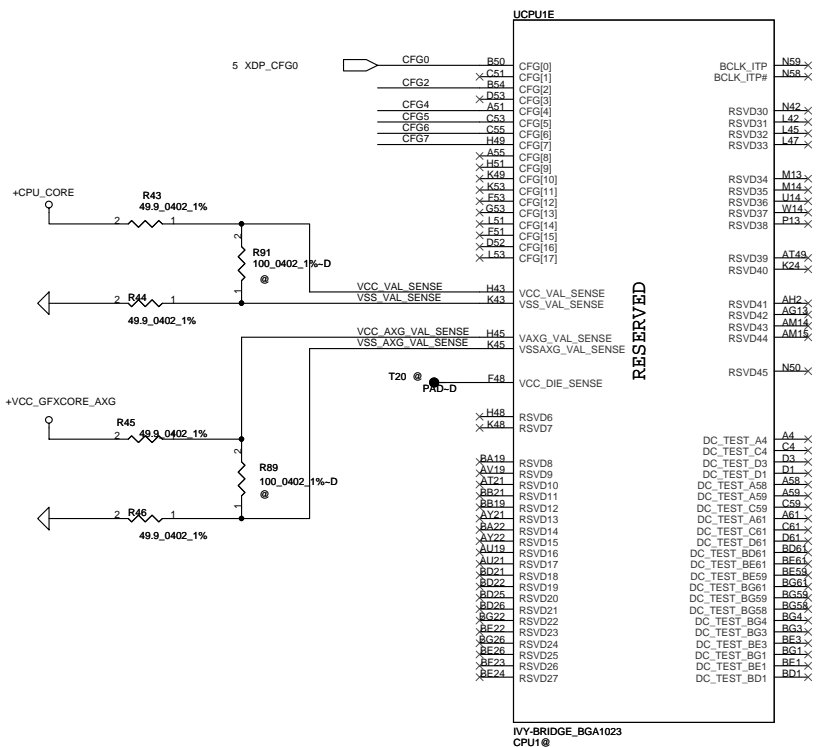
SM Bus Controller 1

Device	Address	HEX
DDR DIMM1		A0
DDR DIMM2		A2
ROM		A8

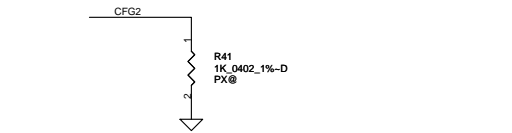
USB3.0	USB2.0	NOTE
1	0	
2	1 *	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	
	5	USB Camera
	6	X
	7	X
	8	
	9 *	WWAN
	10	WLAN
	11	Finger Printer
	12	
	13	BT



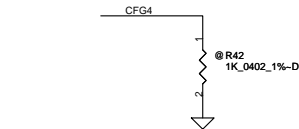




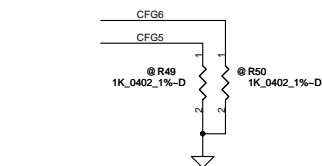
CFG Straps for Processor



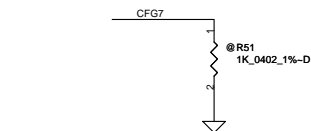
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

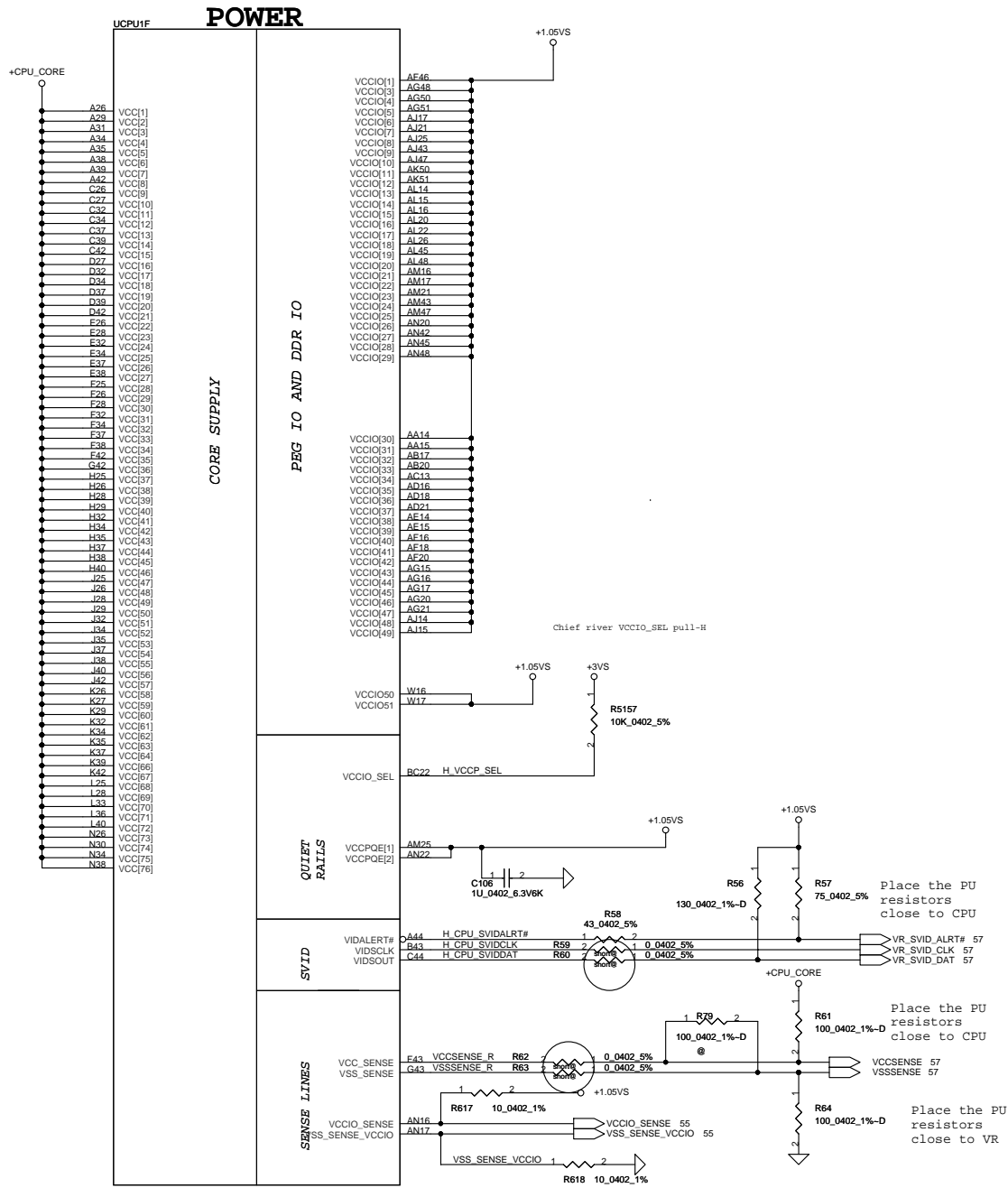


PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU_CORE
GFX_CORE
VCCP1.05

VGA_CORE

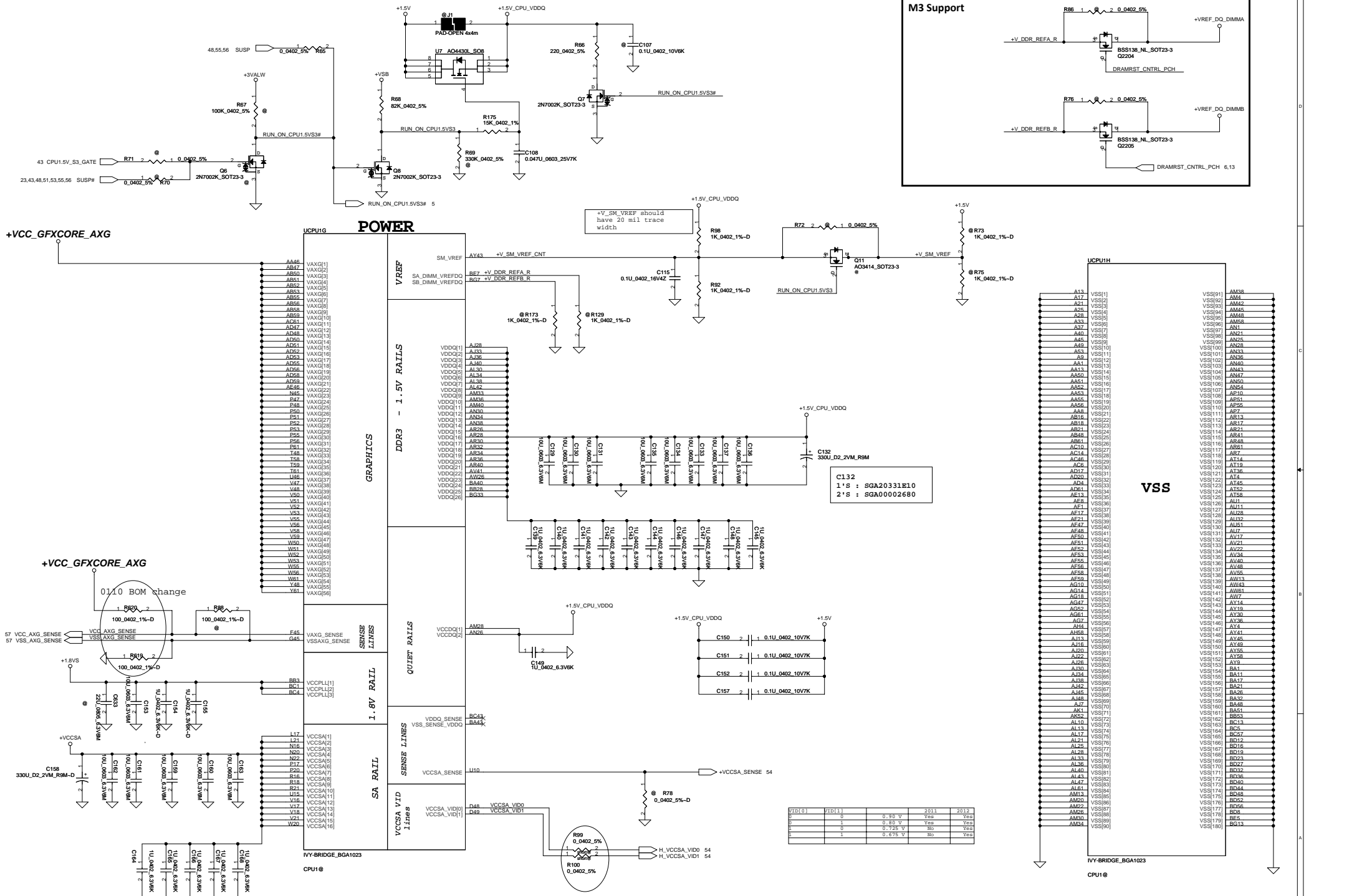
All Capacitor place on Power side.

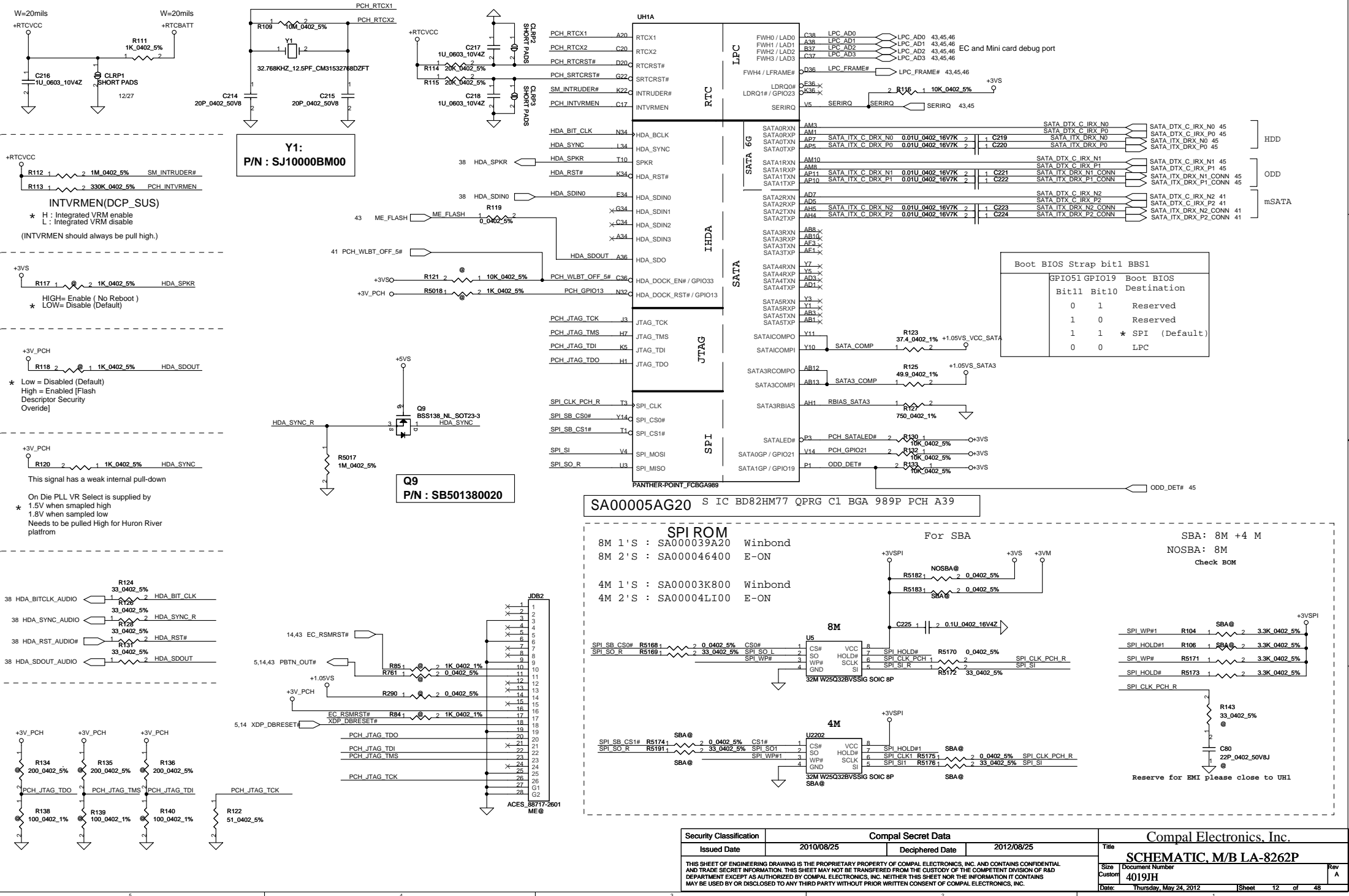


IVY-BRIDGE_BGA1023

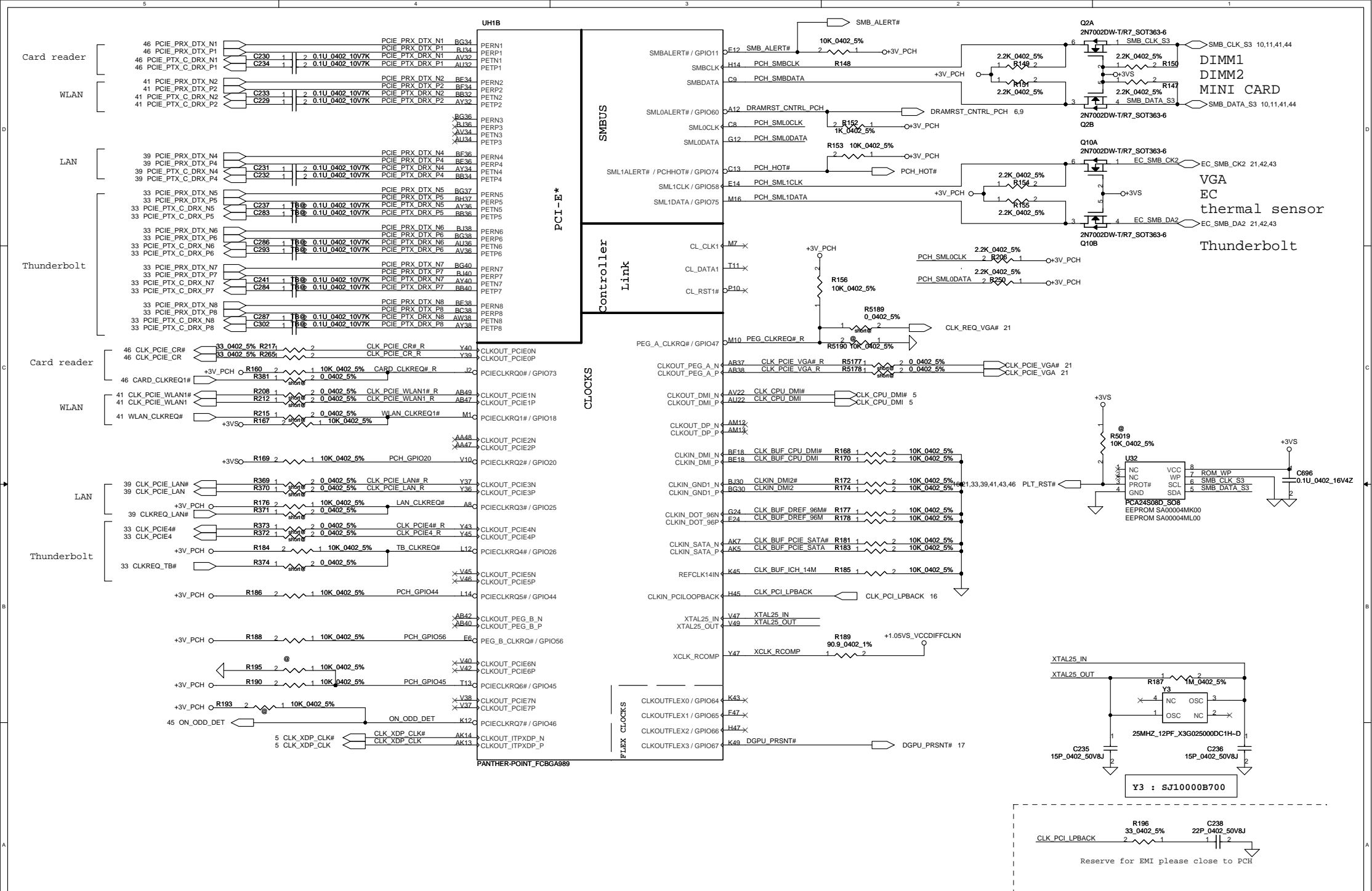
CPU1@

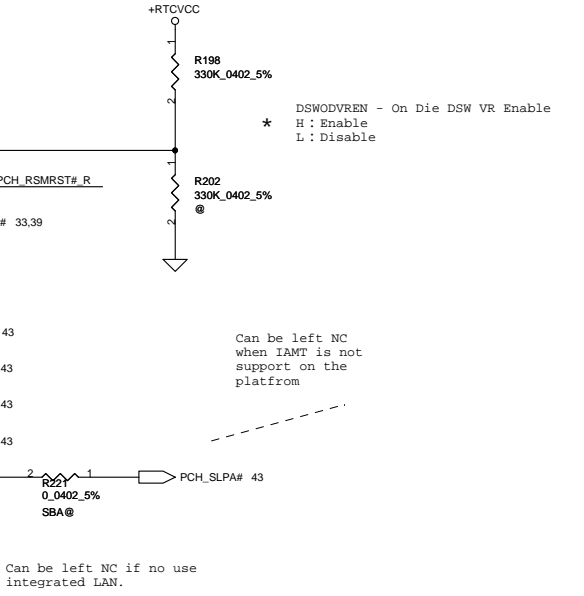
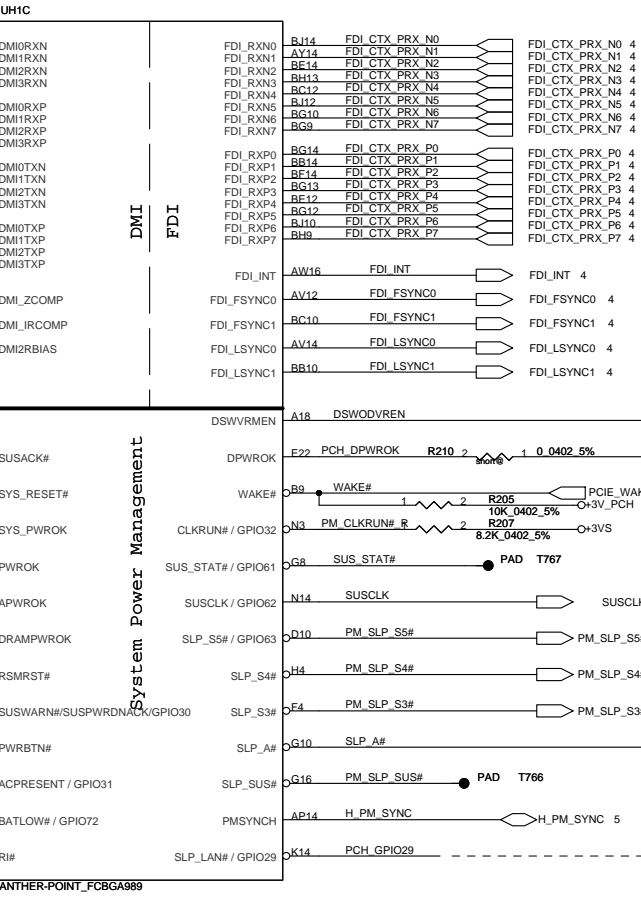
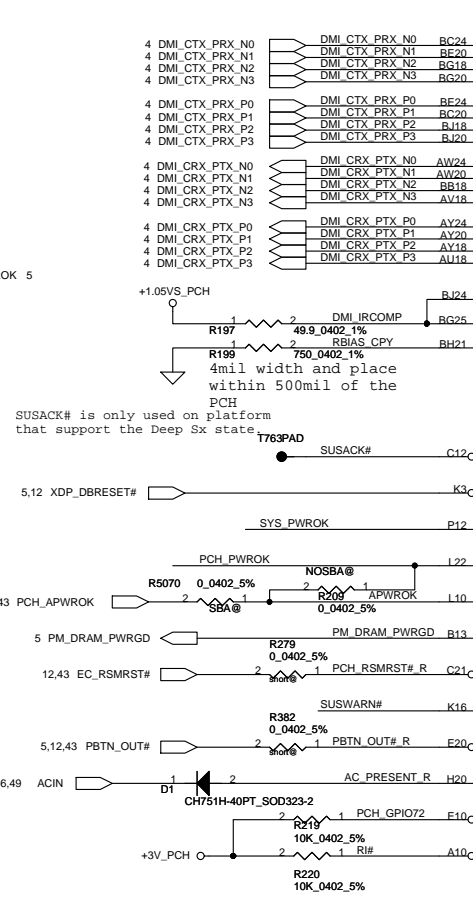
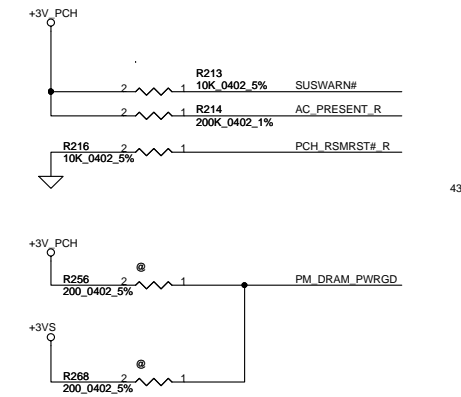
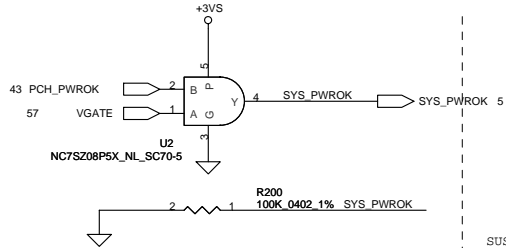
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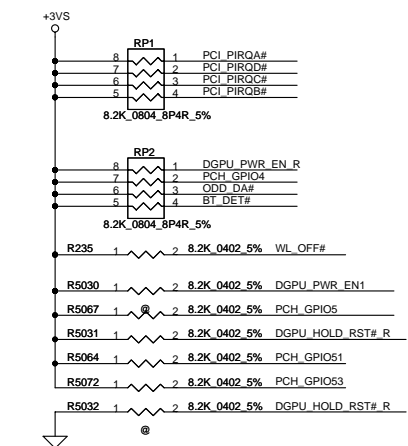


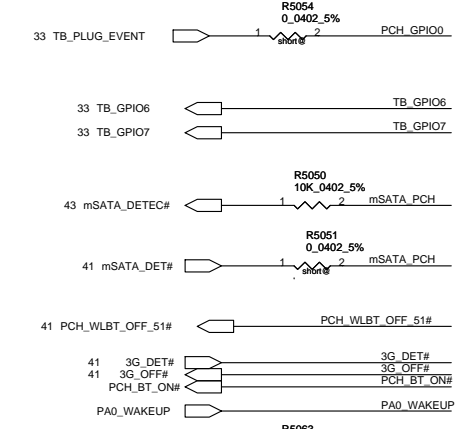
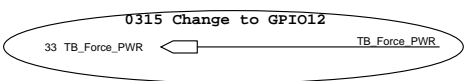
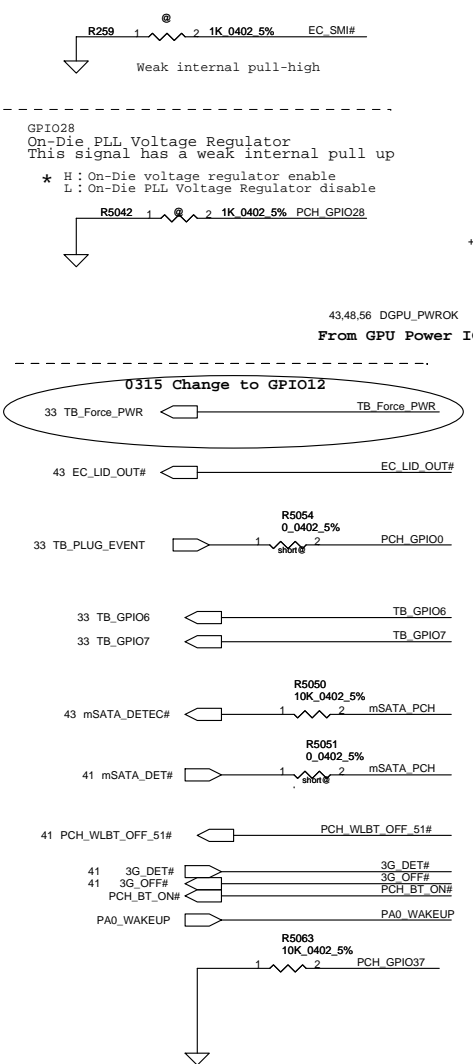


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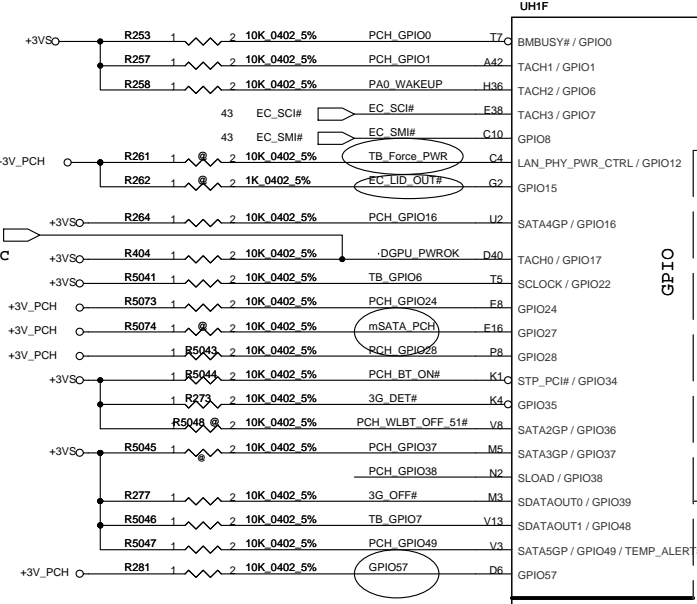
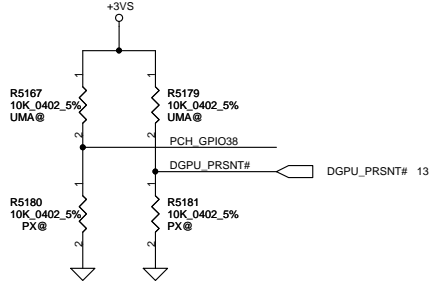




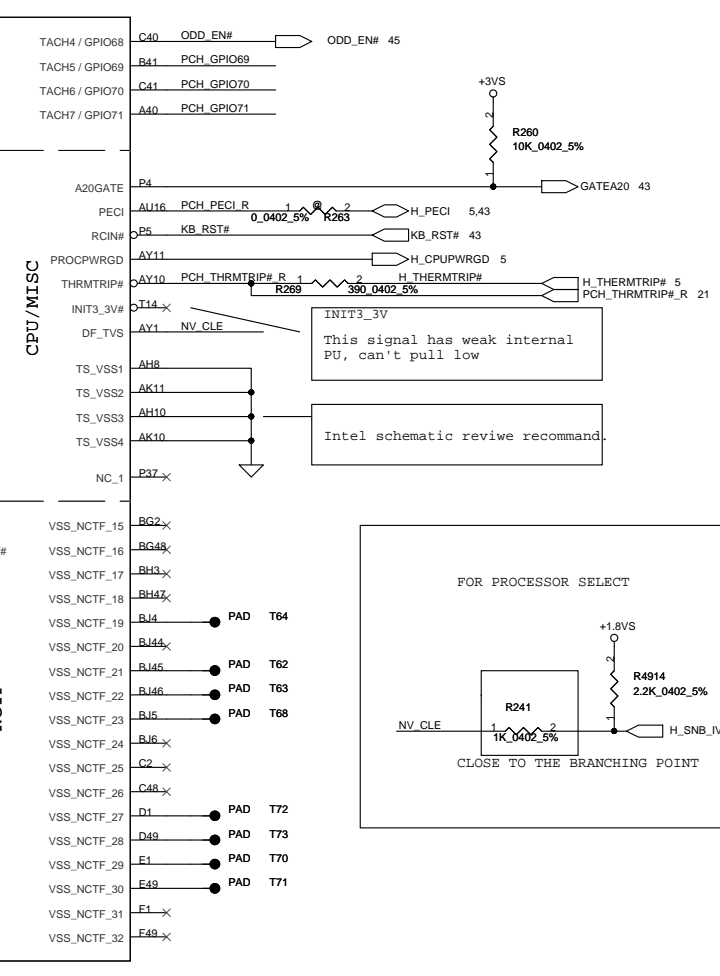
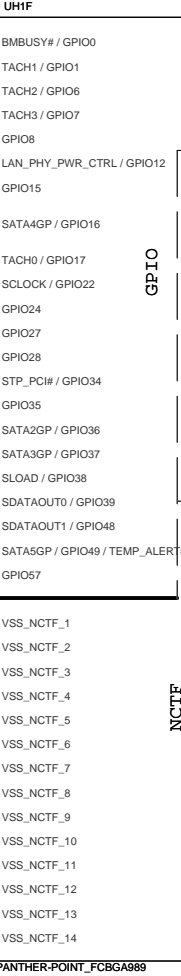
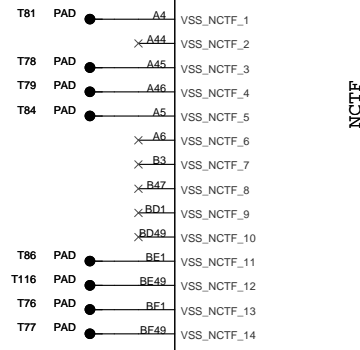




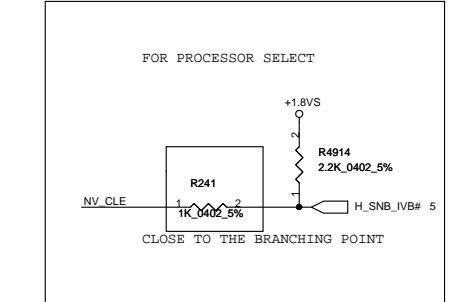
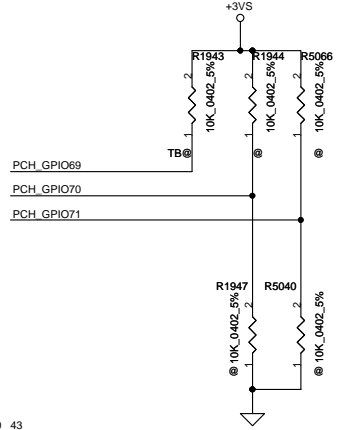
PCH_GPIO38	PCH_GPIO67	Function	GPU_ID
0	0	PX4.0	0
0	1	Reserved	1
1	0	DIS	2
1	1	UMA	3



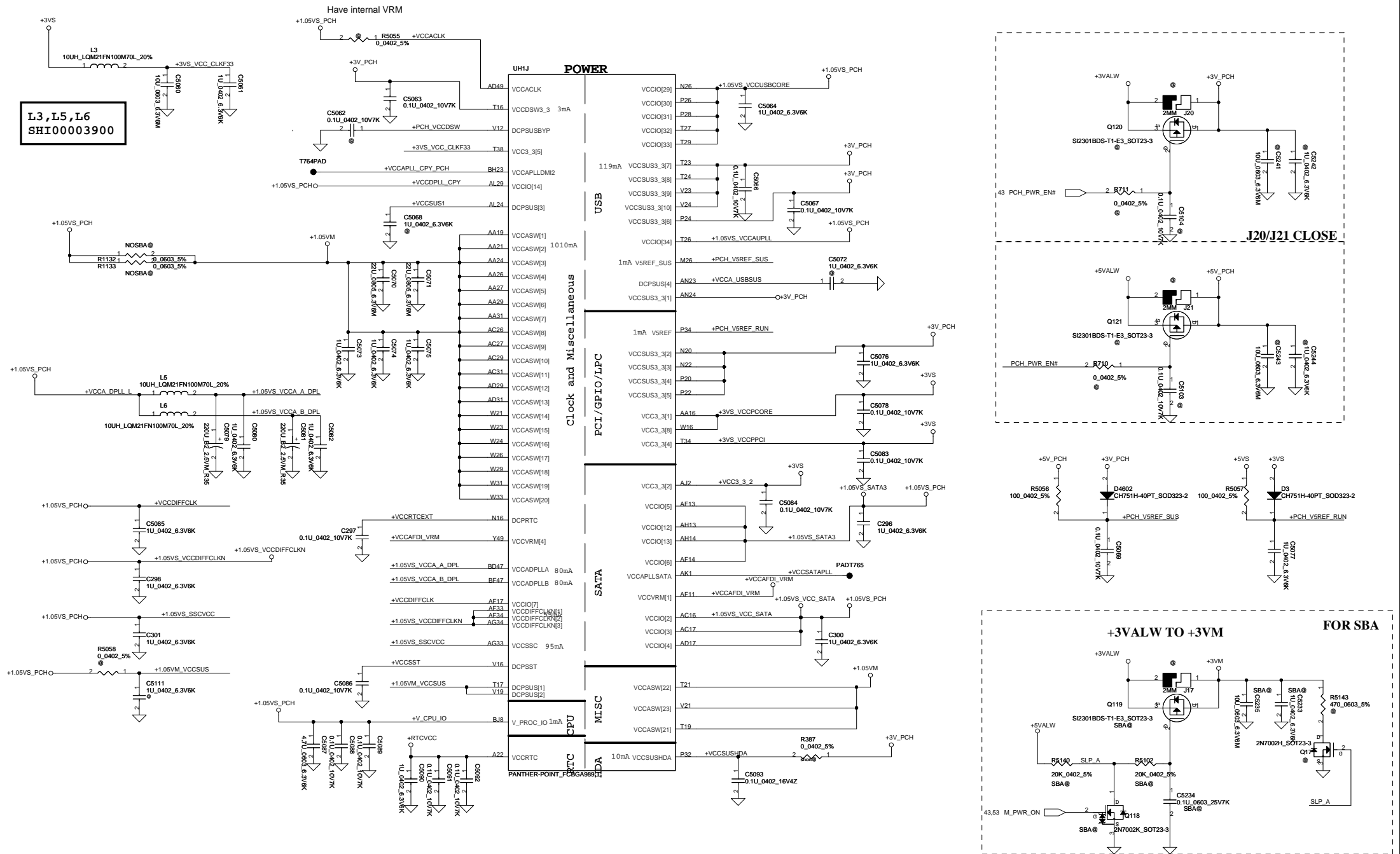
0308
EC_LID_OUT# change to GPIO15
mSATA_PCH change to GPIO27



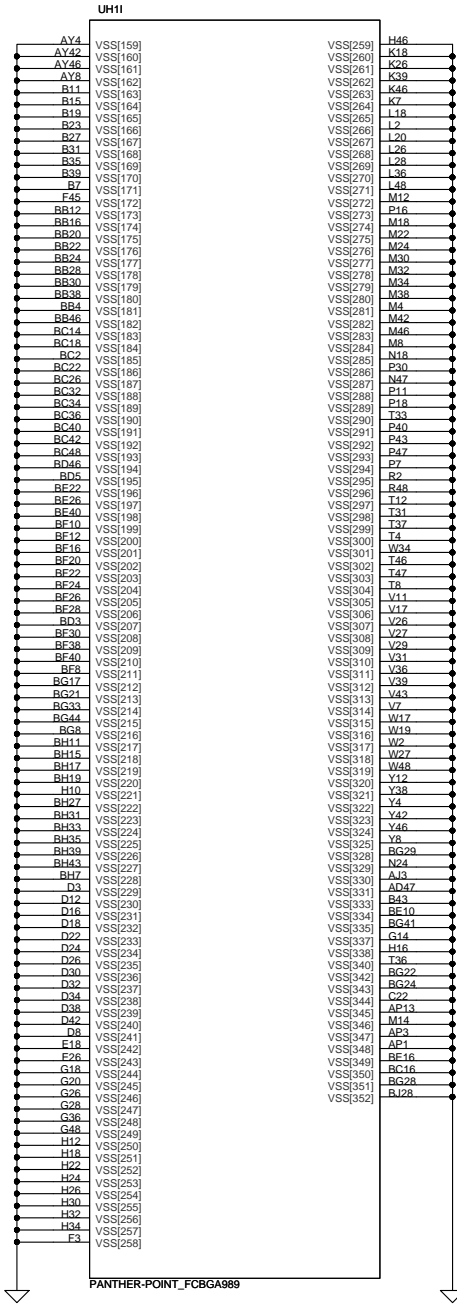
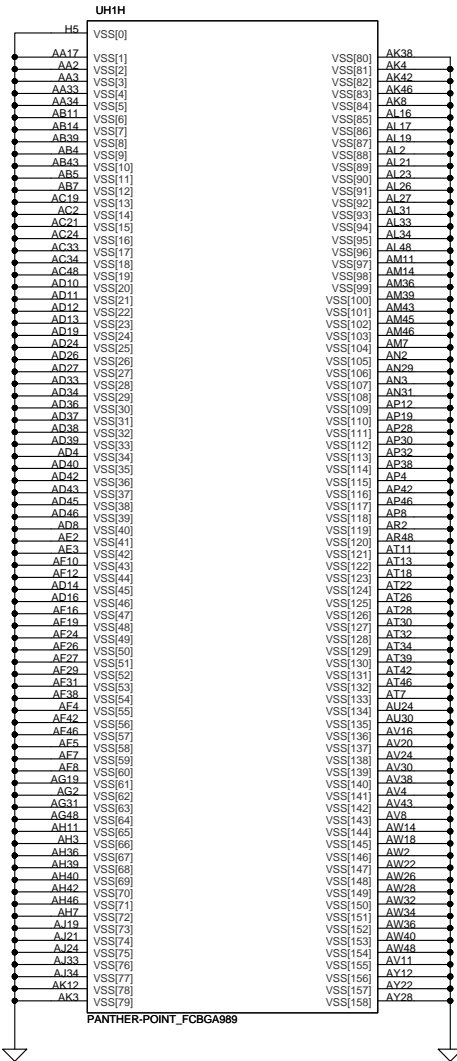
PCH_GPIO69
1 TB SKU
0120 update

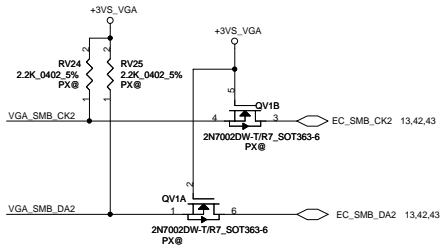
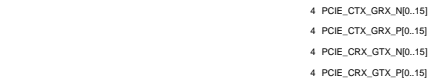


L3,L5,L6
SHI00003900



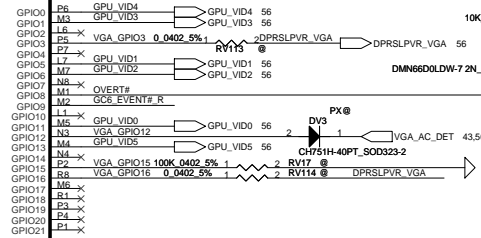
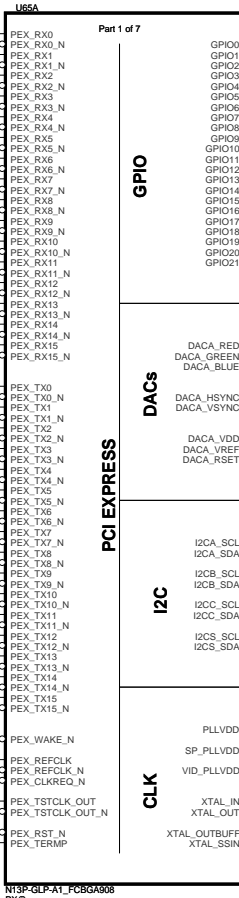
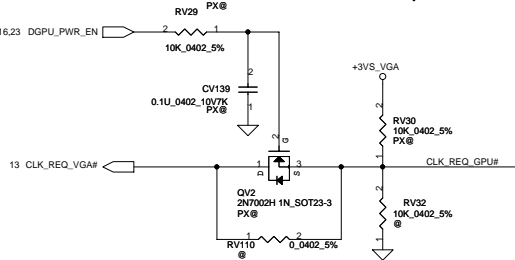
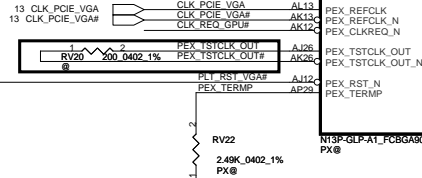
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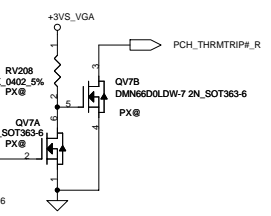
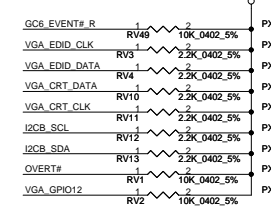


PCIE CRX GTX P0	CV6	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P0	AK14	PEX TX0
PCIE CRX GTX M0	CV7	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N0	AK14	PEX TX0.N
PCIE CRX GTX P1	CV8	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P1	AK14	PEX TX1
PCIE CRX GTX N1	CV9	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N1	AK14	PEX TX1.N
PCIE CRX GTX P2	CV10	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P2	AK15	PEX TX2
PCIE CRX GTX N2	CV11	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N2	AK15	PEX TX2.N
PCIE CRX GTX P3	CV12	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P3	AK16	PEX TX3
PCIE CRX GTX N3	CV13	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N3	AK16	PEX TX3.N
PCIE CRX GTX P4	CV15	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P4	AK17	PEX TX4
PCIE CRX GTX N4	CV17	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N4	AK17	PEX TX4.N
PCIE CRX GTX P5	CV19	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P5	AK17	PEX TX5
PCIE CRX GTX N5	CV14	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N5	AK17	PEX TX5.N
PCIE CRX GTX P6	CV18	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P6	AK18	PEX TX6
PCIE CRX GTX N6	CV18	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N6	AK18	PEX TX6.N
PCIE CRX GTX P7	CV20	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P7	AK19	PEX TX7
PCIE CRX GTX N7	CV22	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N7	AK19	PEX TX7.N
PCIE CRX GTX P8	CV24	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P8	AK20	PEX TX8
PCIE CRX GTX N8	CV26	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N8	AK20	PEX TX8.N
PCIE CRX GTX P9	CV21	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P9	AK20	PEX TX9
PCIE CRX GTX N9	CV23	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N9	AK20	PEX TX9.N
PCIE CRX GTX P10	CV25	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P10	AK21	PEX TX10
PCIE CRX GTX N10	CV27	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N10	AK21	PEX TX10.N
PCIE CRX GTX P11	CV29	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P11	AK22	PEX TX11
PCIE CRX GTX N11	CV31	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N11	AK22	PEX TX11.N
PCIE CRX GTX P12	CV33	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P12	AK23	PEX TX12
PCIE CRX GTX N12	CV35	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N12	AK23	PEX TX12.N
PCIE CRX GTX P13	CV30	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P13	AK24	PEX TX13
PCIE CRX GTX N13	CV32	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N13	AK24	PEX TX13.N
PCIE CRX GTX P14	CV36	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P14	AK24	PEX TX14
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PCIE CRX GTX P15	CV34	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX P15	AK25	PEX TX15
PCIE CRX GTX N15	CV35	1	2	0.1u 0402 10V7K	PX@	PCIE CRX C GTX N15	AK25	PEX TX15.N

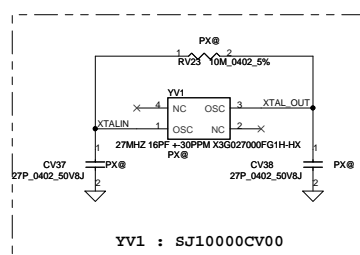
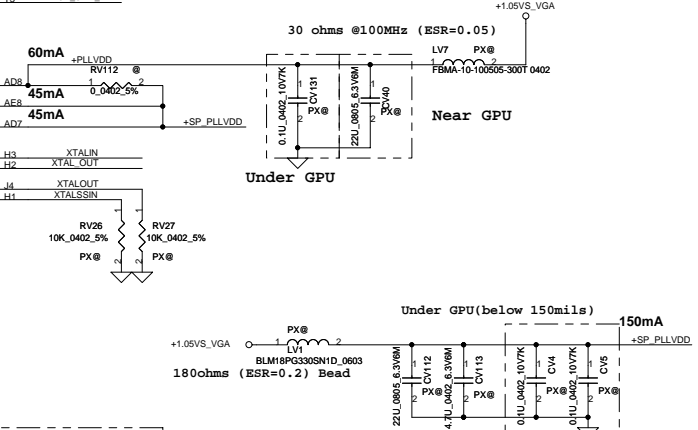
Differential signal
Default leave empty

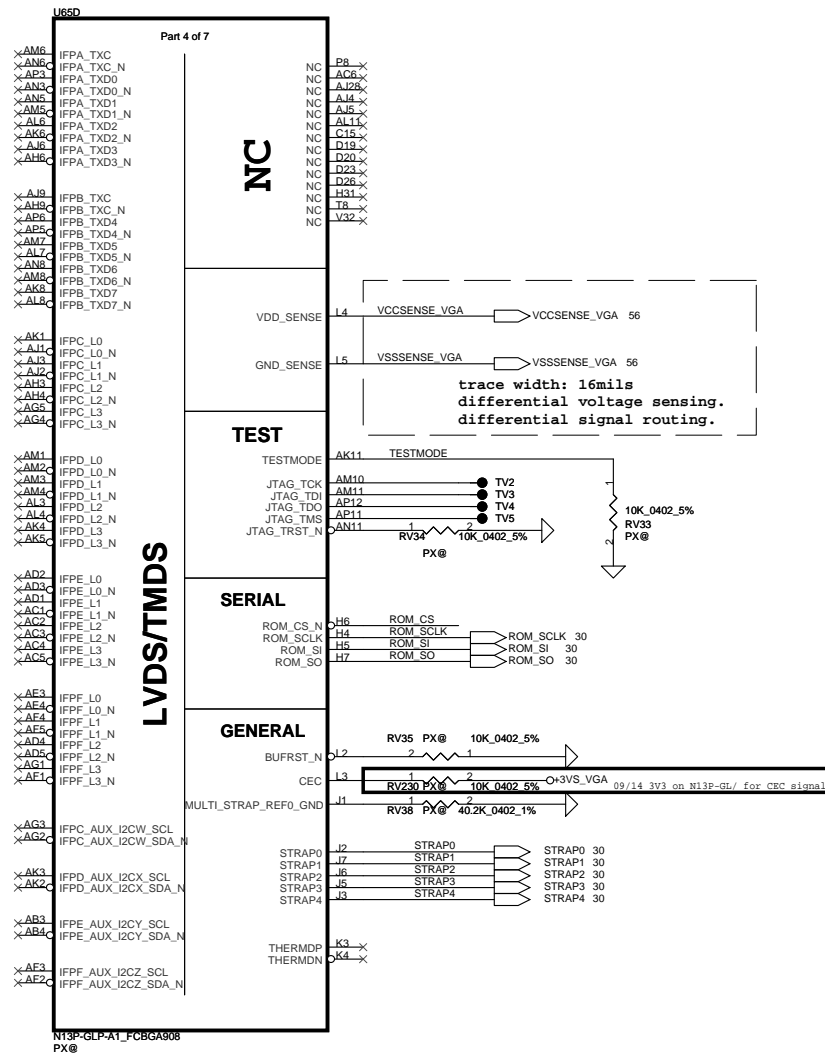


GPIO
DACs
PCI EXPRESS
I2C
CLK

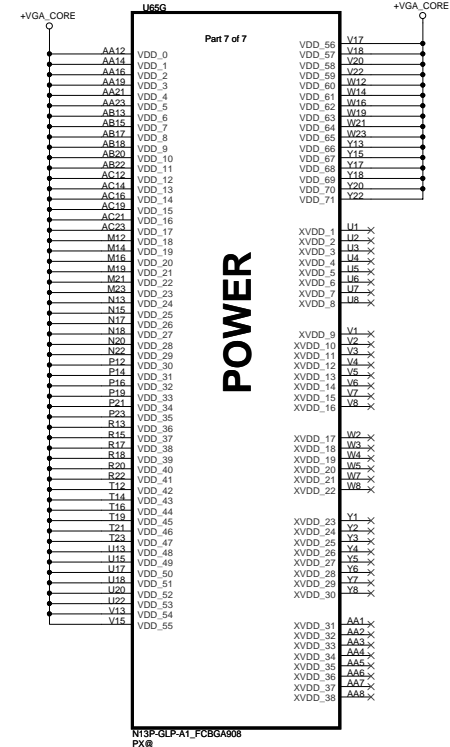
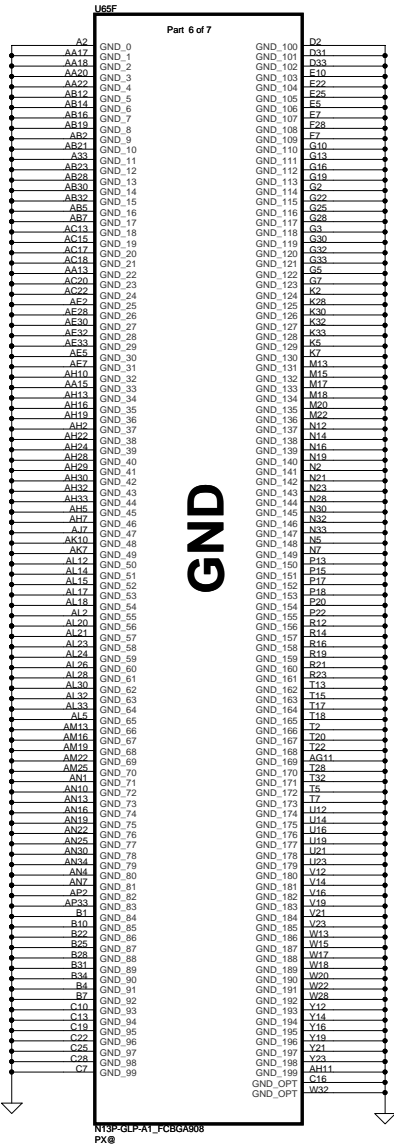


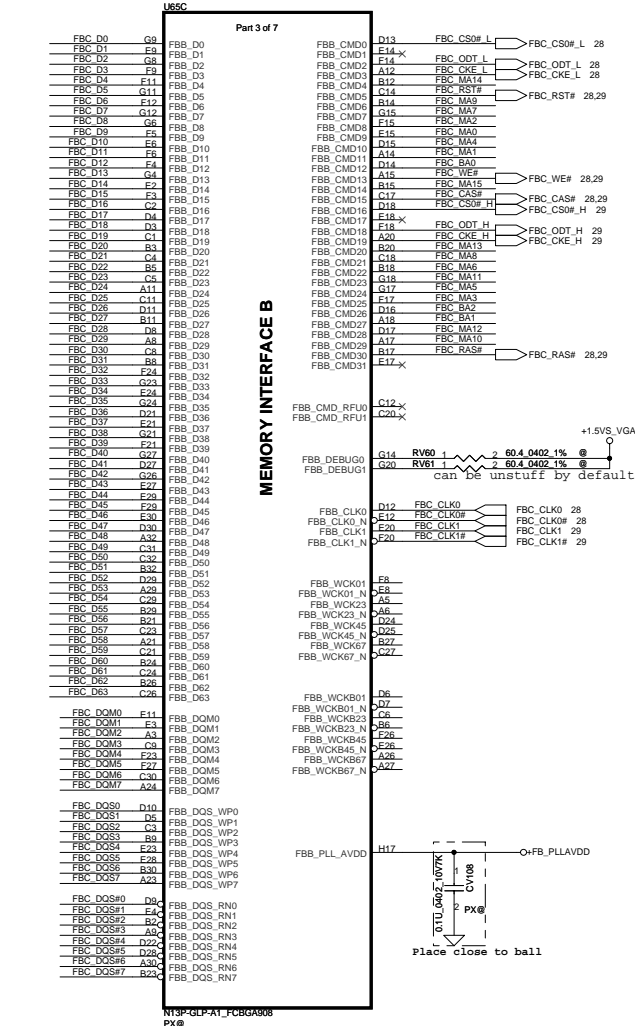
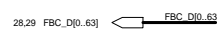
GPIO Pin Name	Internal Function	I/O
GPIO0	GPU_VID0	O
GPIO1	GPU_VID3	O
GPIO2	LCD_BL_PWM	O
GPIO3	LCD_VCC of PSI	O
GPIO4	LCD_BLEN	O
GPIO5	GPU_VID1	O
GPIO6	GPU_VID2	O
GPIO7	3D Vision	O
GPIO8	OVERI	I/O
GPIO9	ALERT	I/O
GPIO10	MEM_VREF_CTL	O
GPIO11	GPU_VID5	O
GPIO12	PWR_LEVEL	I
GPIO13	GPU_VID6	O
GPIO14	HPD_AB	I
GPIO15	HPD_C	I
GPIO16	PSI or MEM_VDD_CTL	O
GPIO17	HPD_D	I
GPIO18	HPD_E	I
GPIO19	HPD_F	I
GPIO20	RSV	O
GPIO21	RSV	O





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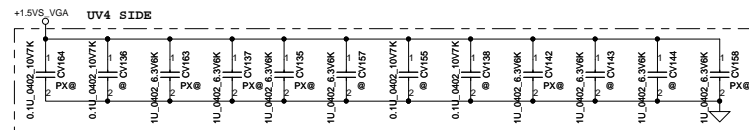
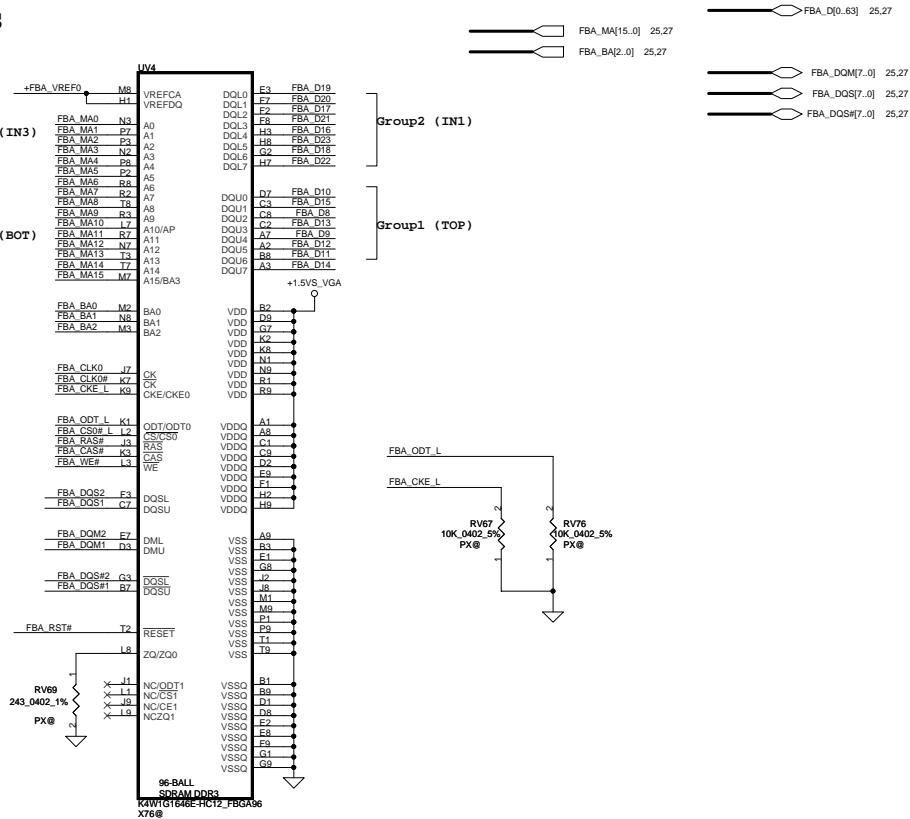
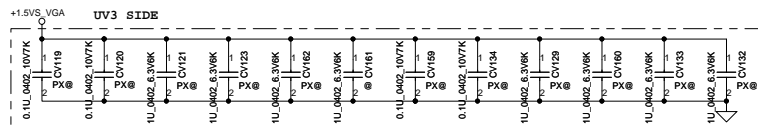


	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS0#_L	
FBX_CMD1		
FBX_CMD2	ODT_L	
FBX_CMD3	CKE_L	
FBX_CMD4	A14	A14
FBX_CMD5	RST	RST
FBX_CMD6	A9	A9
FBX_CMD7	A7	A7
FBX_CMD8	A2	A2
FBX_CMD9	A0	A0
FBX_CMD10	A4	A4
FBX_CMD11	A1	A1
FBX_CMD12	BA0	BA0
FBX_CMD13	WE#	WE#
FBX_CMD14	A15	A15
FBX_CMD15	CAS#	CAS#
FBX_CMD16	CS0#_	
FBX_CMD17		
FBX_CMD18		ODT_H
FBX_CMD19		CKE_H
FBX_CMD20	A13	A13
FBX_CMD21	A8	A8
FBX_CMD22	A6	A6
FBX_CMD23	A11	A11
FBX_CMD24	A5	A5
FBX_CMD25	A3	A3
FBX_CMD26	BA2	BA2
FBX_CMD27	BA1	BA1
FBX_CMD28	A12	A12
FBX_CMD29	A10	A10
FBX_CMD30	RAS#	RAS#

28,29 FBC_DQM[7..0]

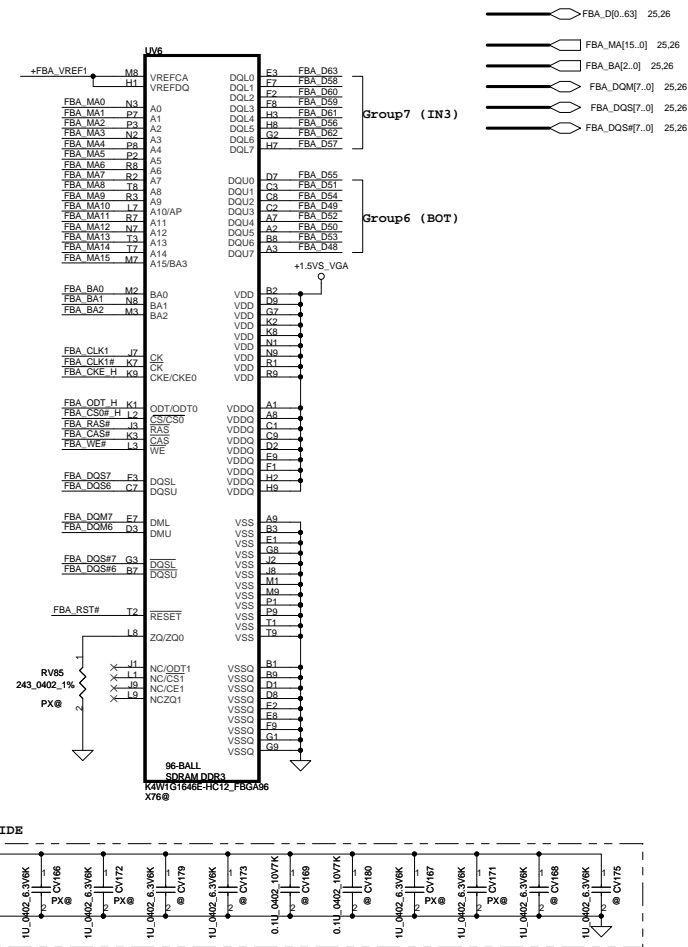
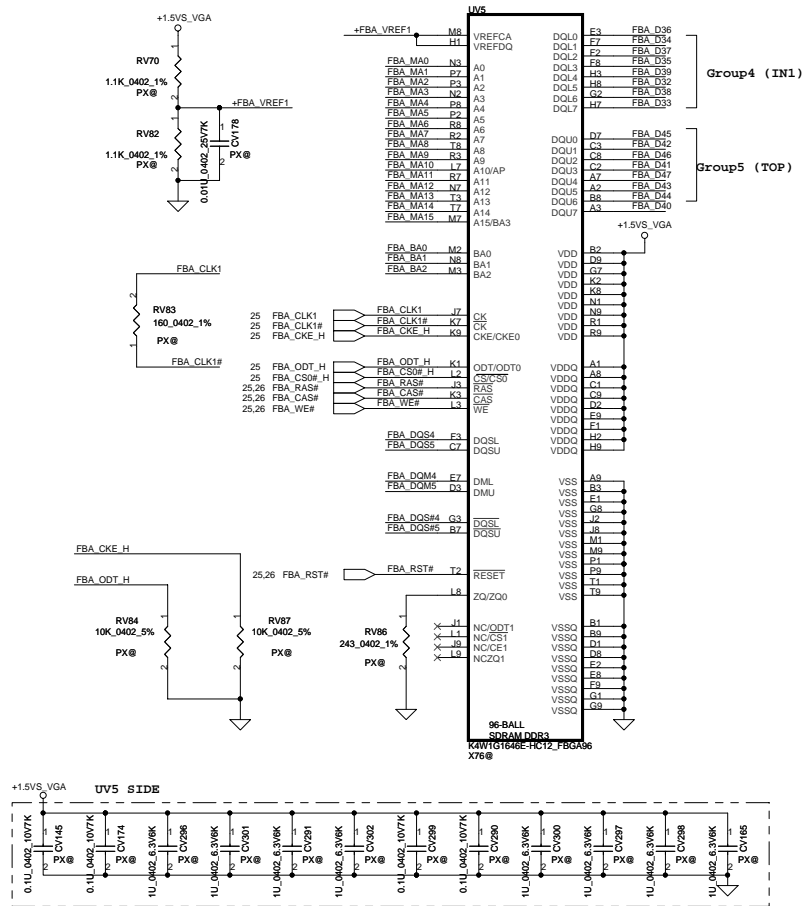
28,29 FBC_DQS[7..0]

28,29 FBC_DQS# [7..0] 

[illegible]

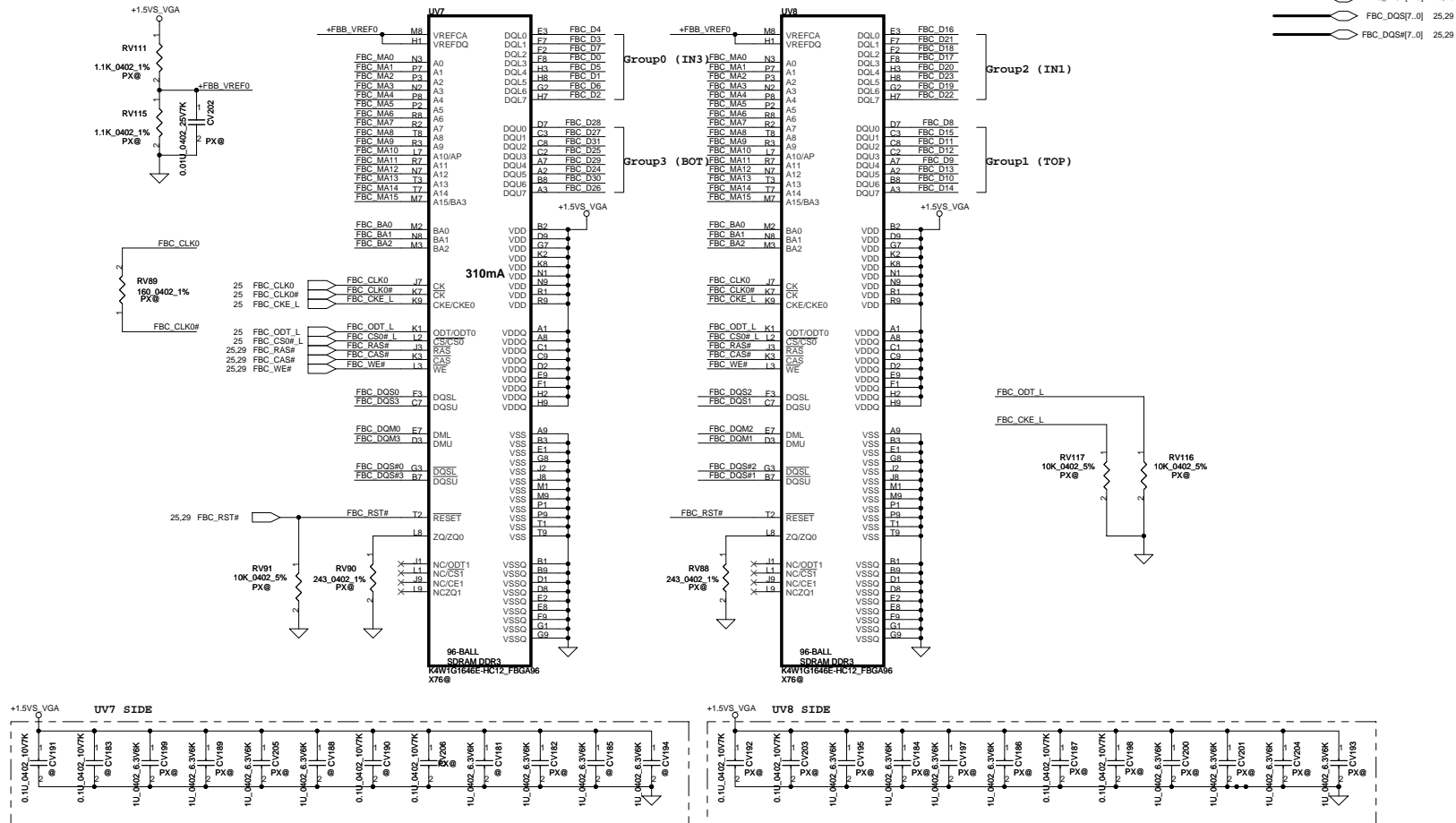
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Memory Partition A - Upper 32 bits



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				Date:	Thursday, May 24, 2012	Sheet

Memory Partition C - Lower 32 bits

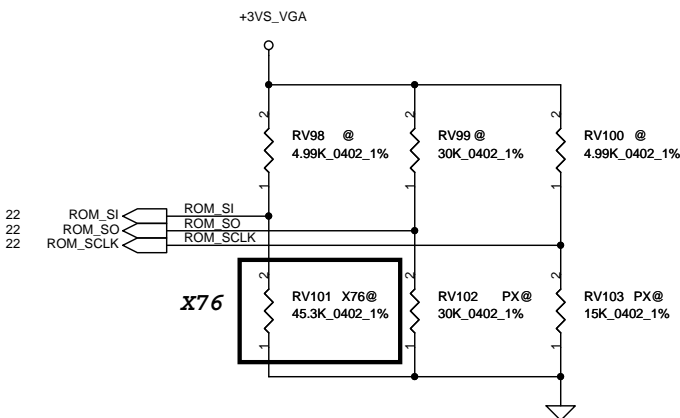
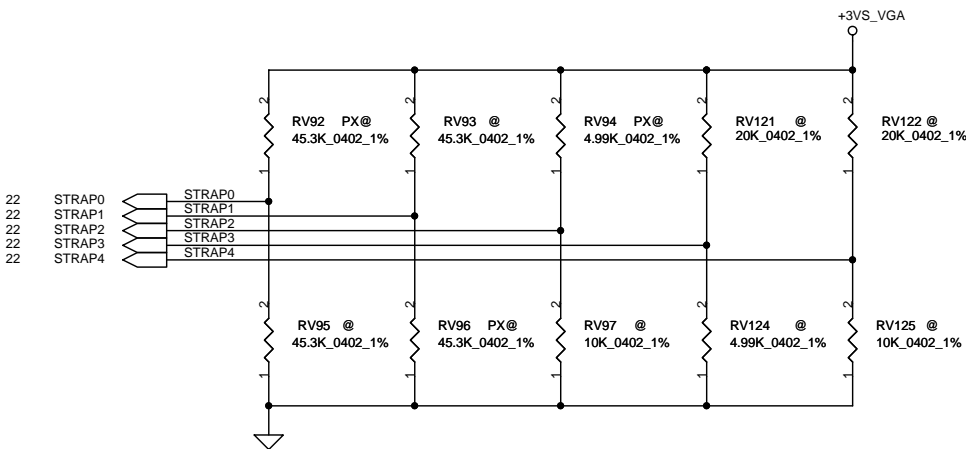


FBC_D[0.63] 25,29
FBC_MA[15.0] 25,29
FBC_BA[2.0] 25,29
FBC_DQM[7.0] 25,29
FBC_DQS[7.0] 25,29
FBC_DQS# [7.0] 25,29

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A diagram of a horizontal bar divided into four segments labeled A, B, C, and D from left to right. Segment A is the shortest, followed by B, then C, and D is the longest. A vertical line with an arrow points to the boundary between segments B and C.





For N13P-GLP strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GLP	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	RV92 PU 45K	RV96 PD 45K	RV94 PU 5K	N/A	N/A	RV101 PD 45K	RV102 PD 30K	RV103 PD 15K
	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ1G63DFR-11C	RV92 PU 45K	RV96 PD 45K	RV94 PU 5K	N/A	N/A	RV101 PD 35K	RV102 PD 30K	RV103 PD 15K

X76

RV101 X76@
34.8K_0402_1%
SD034348280

ZZZ
Samsung
S2G@
X7636539L02

ZZZ
Hynix
H2G@
X7636539L01

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	0110 Notebook Default

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

XCLK_417	
0	277MHz (Default)
1	Reserved

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps	
User[3:0]	1000-1100 Customer defined

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

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		4019JH							
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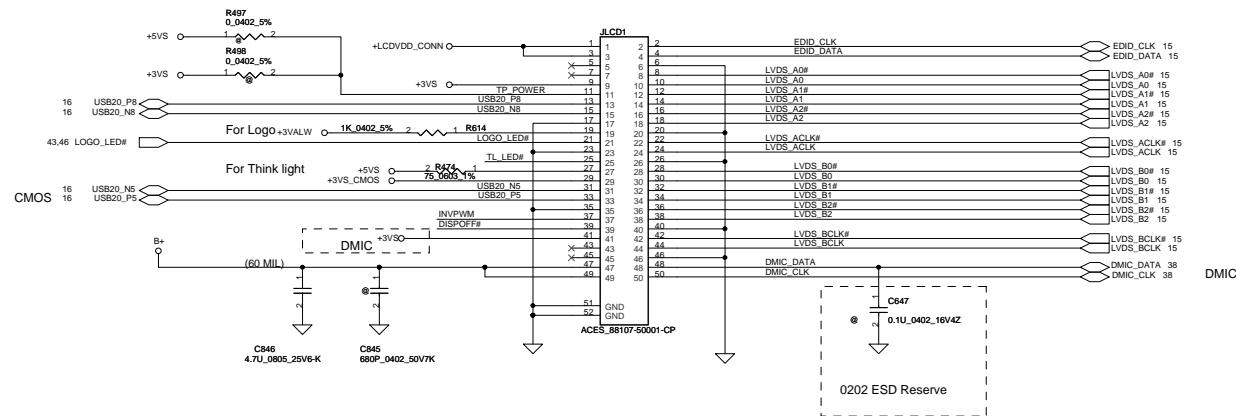
USB20_N8

USB20_P8

D38

PUDLC05_SOT23-3

SCA00000U10



15 PCH_EN/VD

15 PCH_PWM

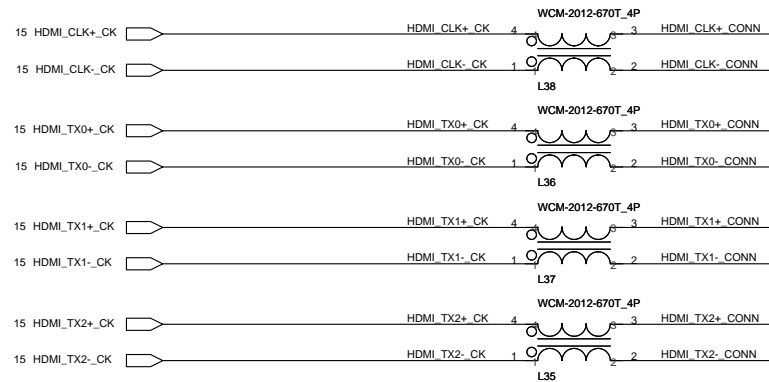
43 BKOFF#

DISOFF#

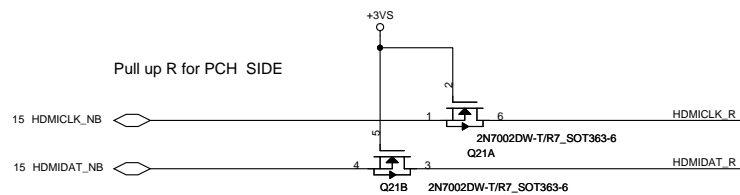
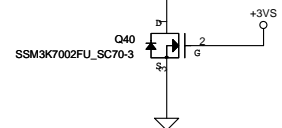
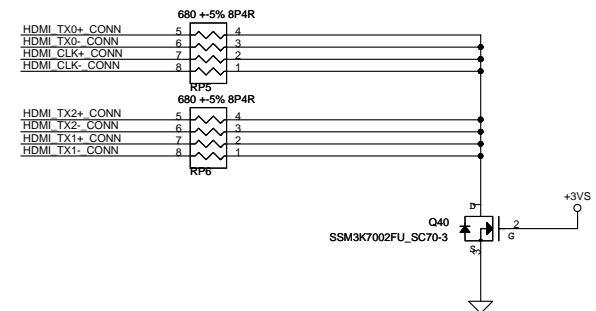
For GMCH DPST

The schematic diagram, titled "CMOS Camera Conn", illustrates the electrical connection for a camera module. It features a 3V3O power supply line (20 MIL) connected to the VCC pin (pin 1) of a component labeled Q35, S2301BDS-T1-E3_SOT23-3. A 4.7V resistor (R451, 150K_0402_5%) is connected between the CMOS_ON# signal line (pin 43) and the GND pin (pin 4) of the component. A 0.1uF_0402_16V4Z capacitor (C644) is connected between the GND pin and the common ground. Additionally, a 3V3V_CMOS supply line is connected to the VCC pin (pin 8) of the component, with a 0.1uF_0402_16V4Z capacitor (C642) and a 10uF_0603_6.3V6M capacitor (C643) connected to ground for decoupling. The component is also connected to a common ground (pin 7).

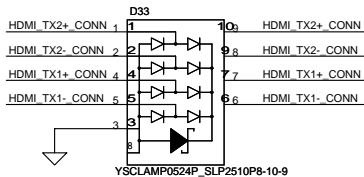
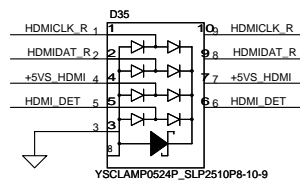
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Size	Document Number			Rev A	
Custm				4019JH	
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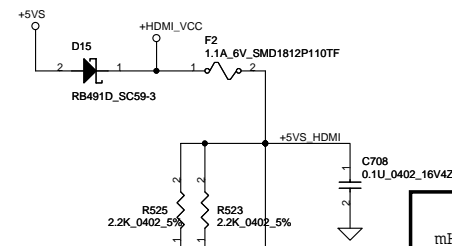
L35, L36, L37, L38
S COM FI_ KINGCORE WCM-2012HS-900T
P/N : SM070001S00



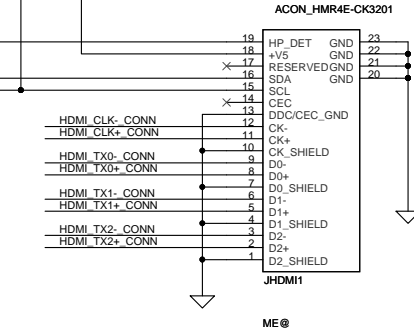
Pull up R for PCH SIDE



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2'SPN: SC300002800

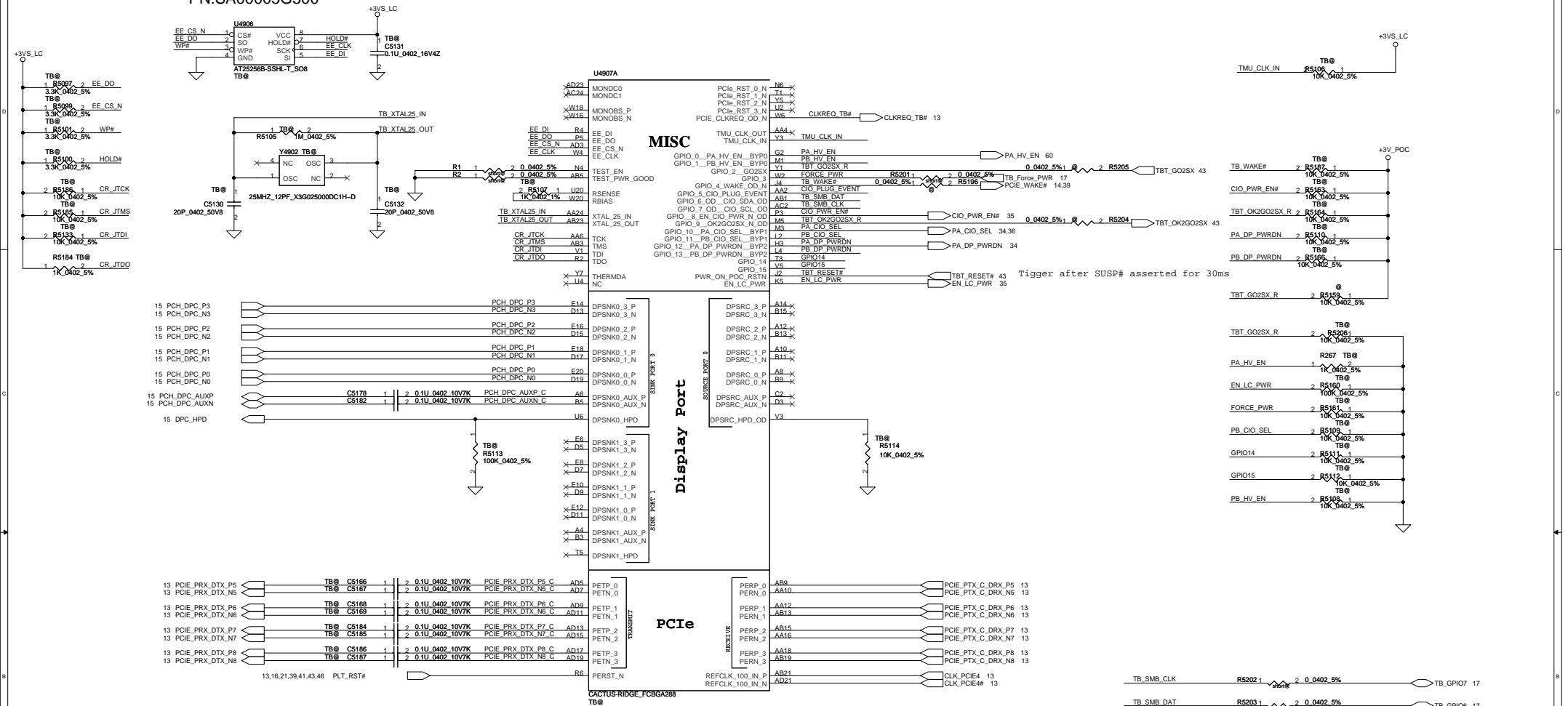


TYPE C Connector
mHDMI PN:SP060005H00



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						Size		Document Number		Rev					
						Custom		4019JH		A					
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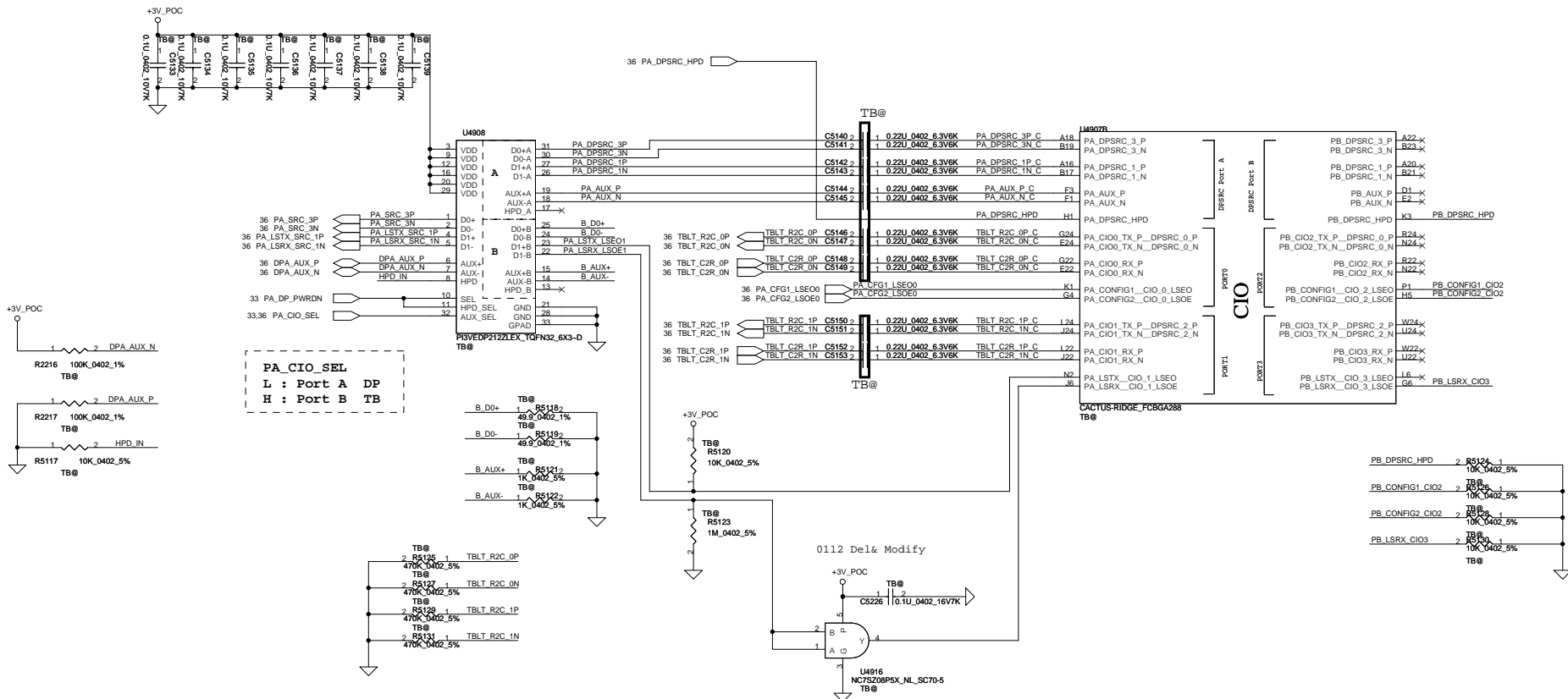
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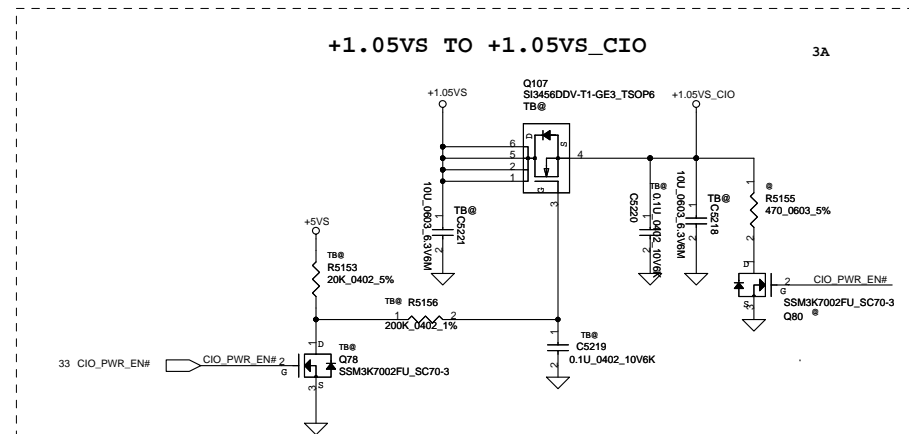
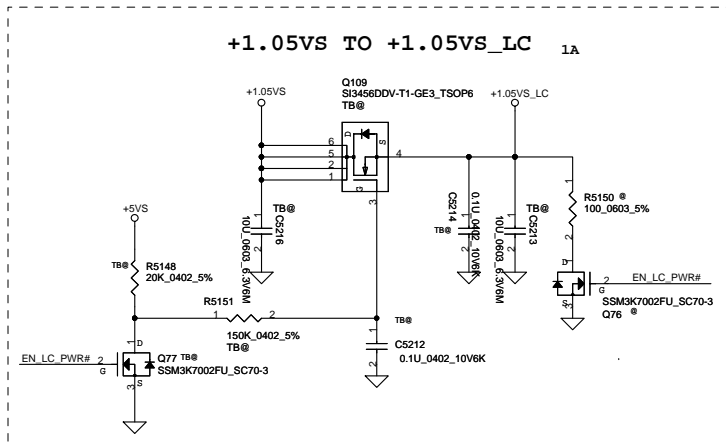
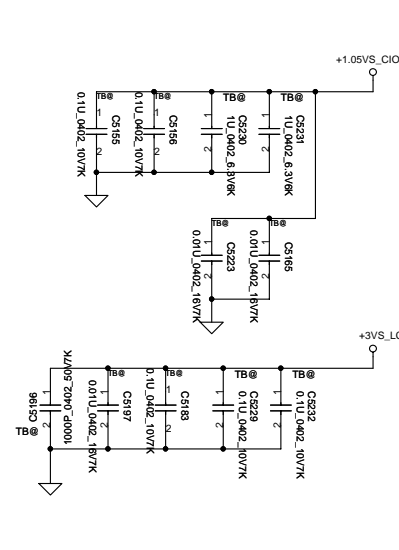


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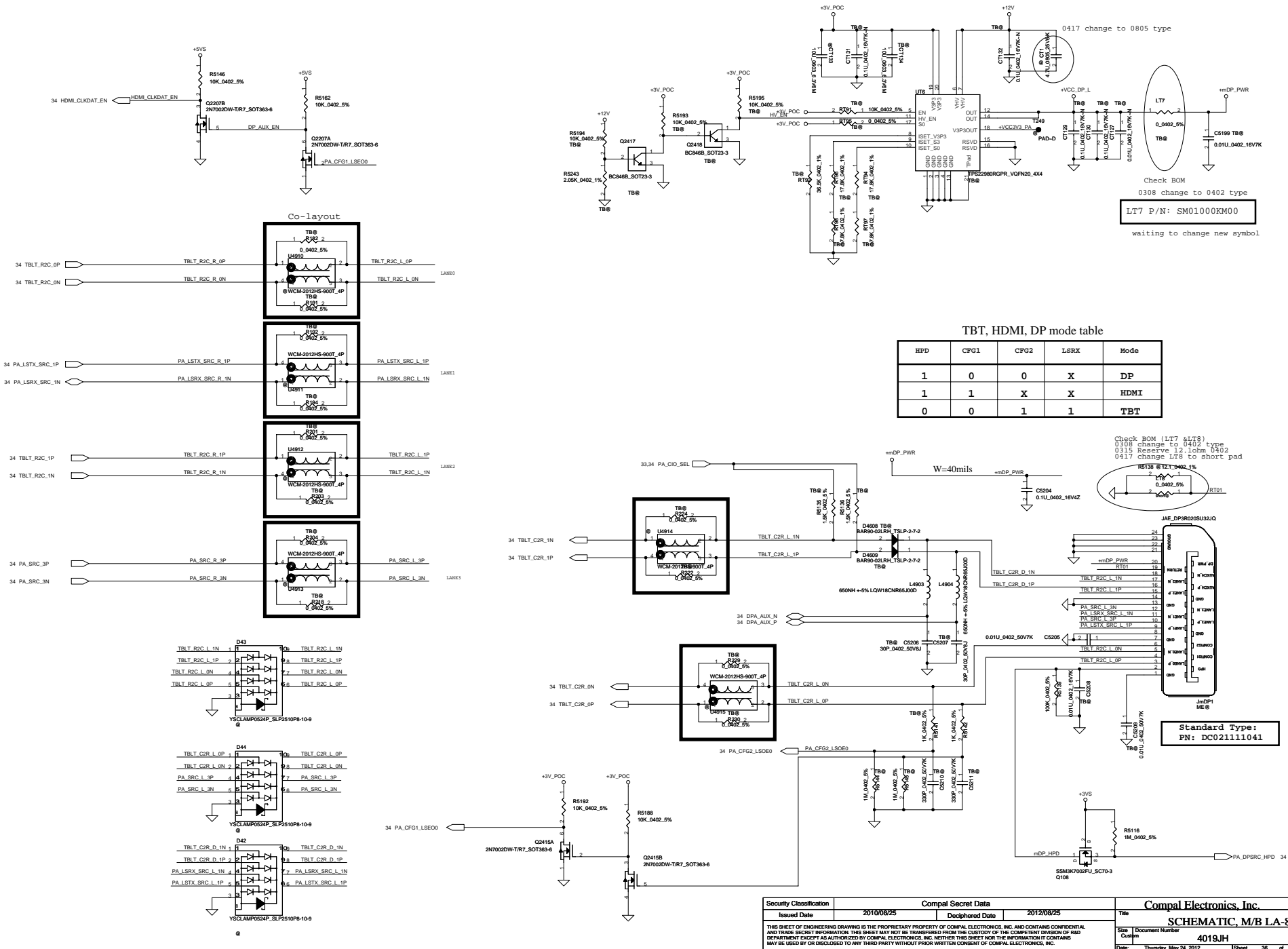
0112 Modify

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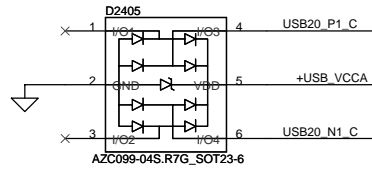
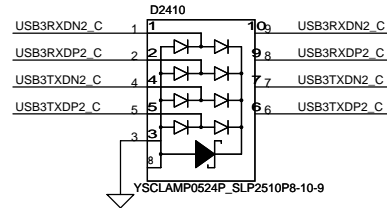


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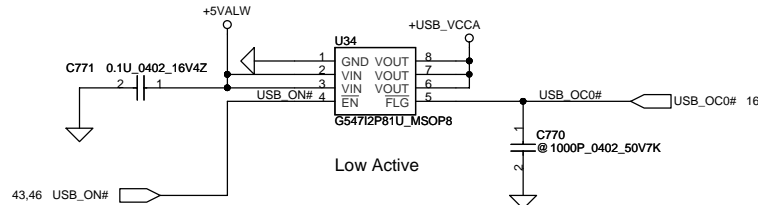


HPD	CFG1	CFG2	LSRX	Mode
1	0	0	X	DP
1	1	X	X	HDMI
0	0	1	1	TBT

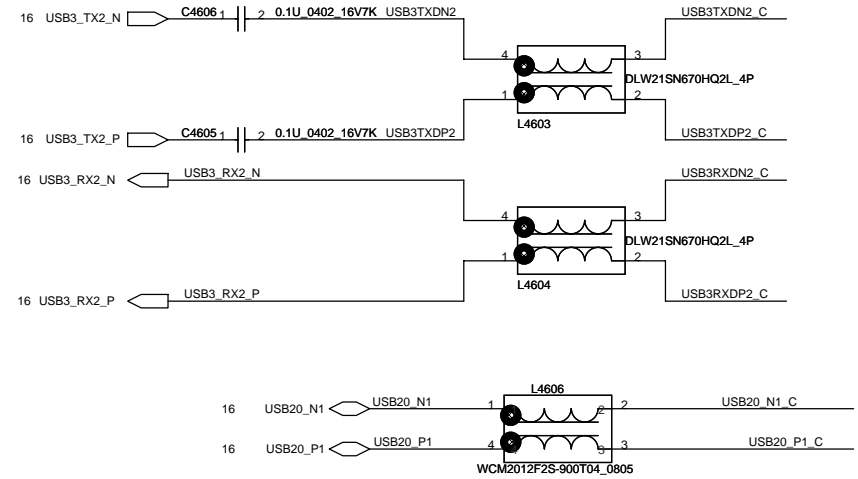
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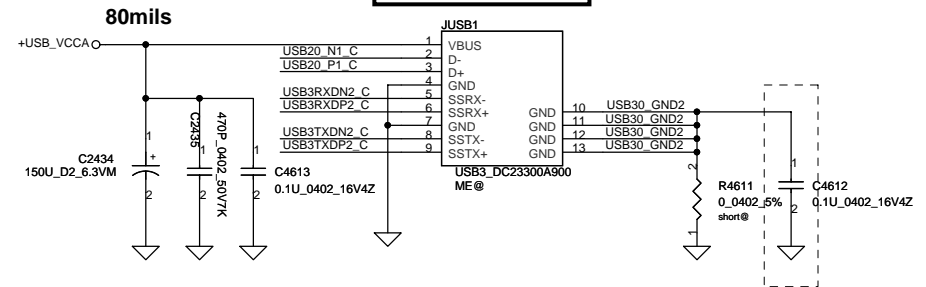


JUSB1USB3.0/USB2.0



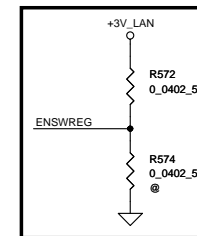
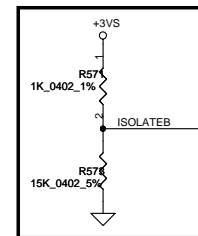
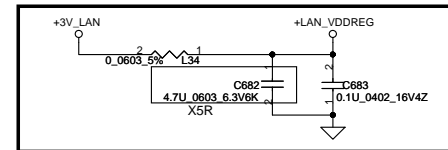
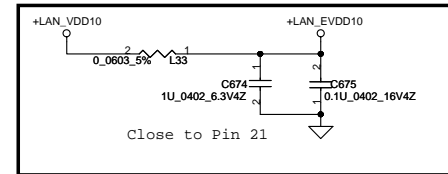
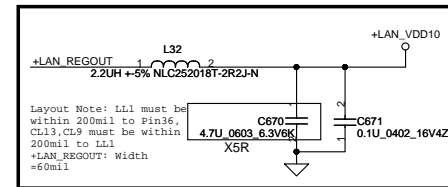
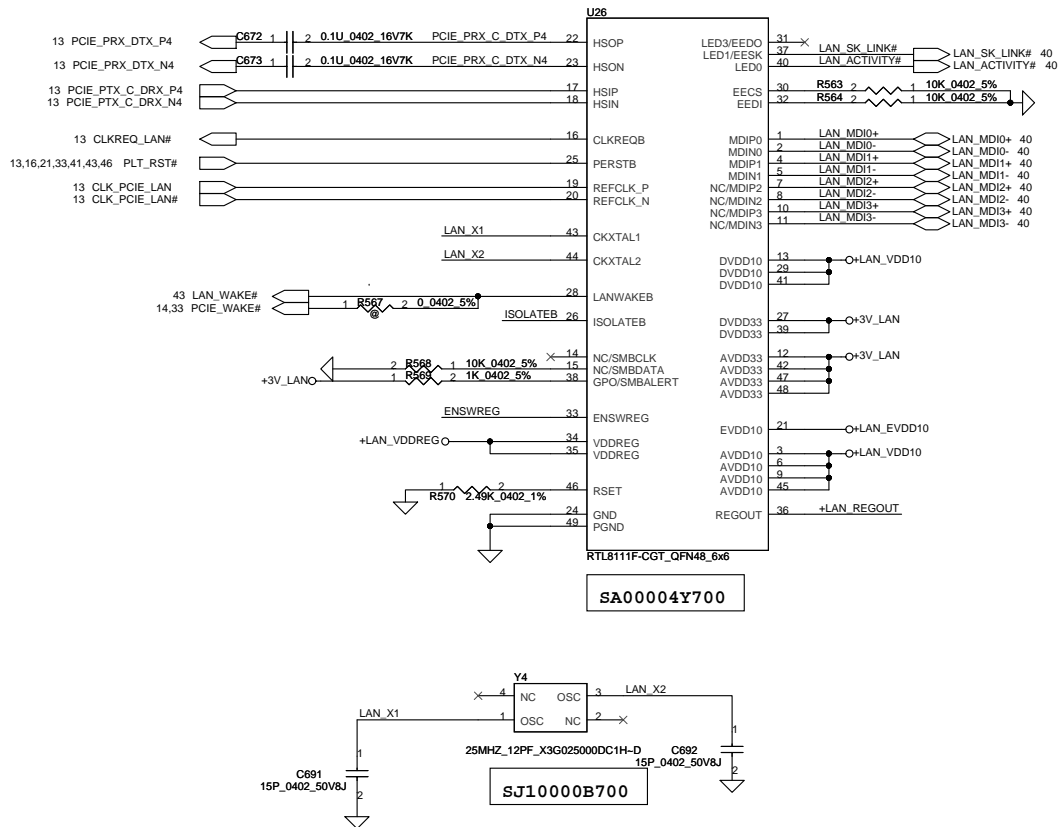
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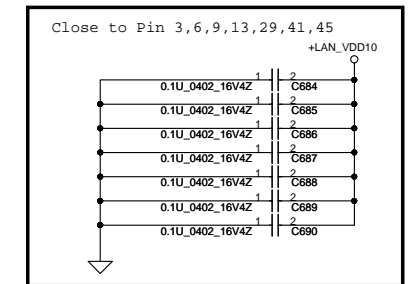
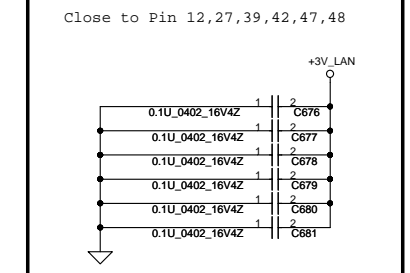
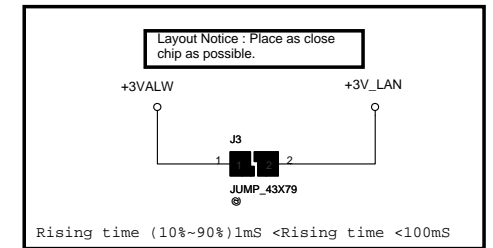


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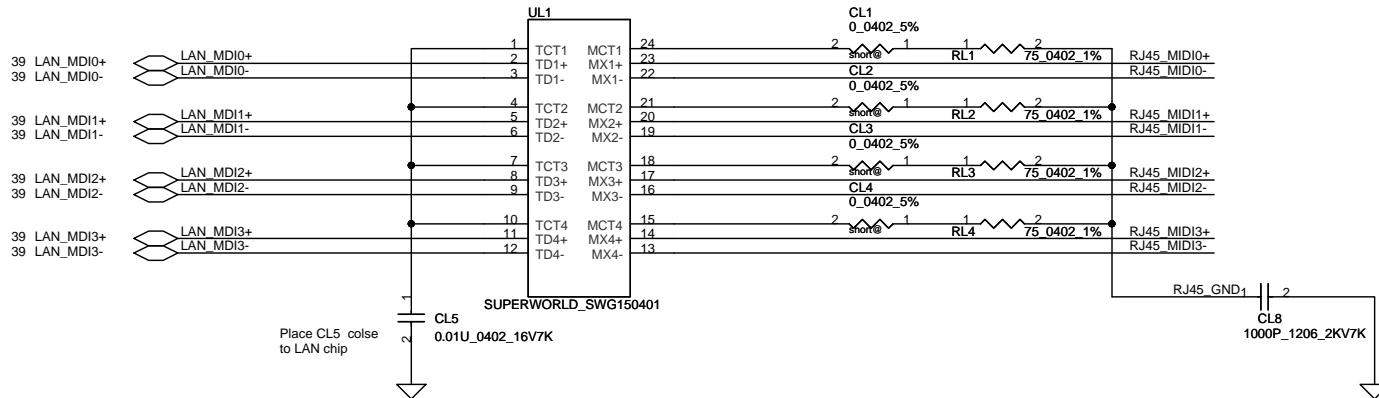


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L: Disable

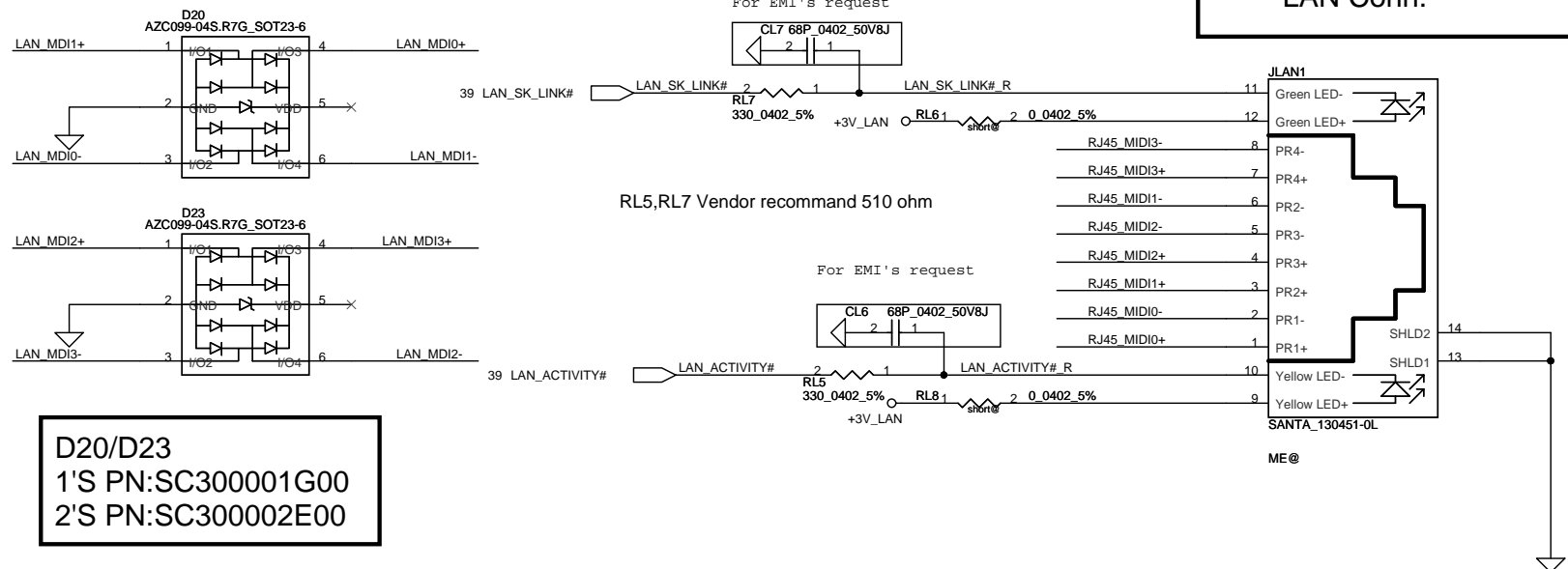


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SP050006F00



DC23111211
LAN Conn.



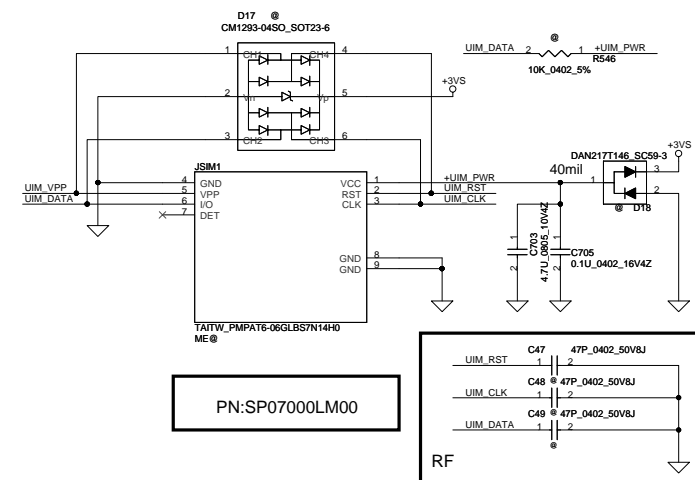
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Mini-Express Card(WLAN/WiMAX)

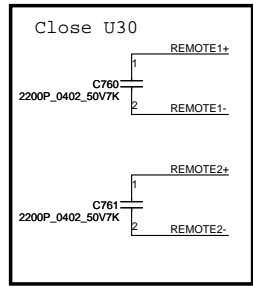


0131 remove BT

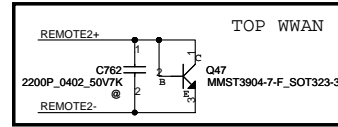
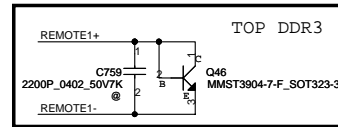
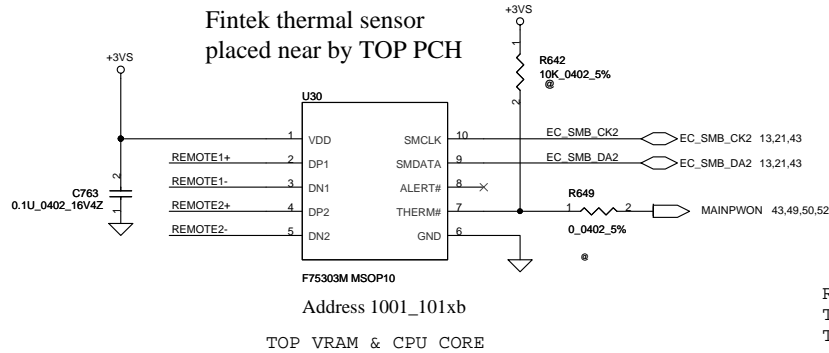
For AOAC assessment 11/09 add AOAC function.



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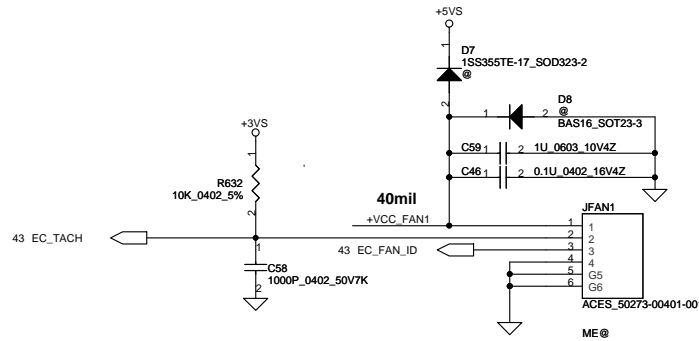
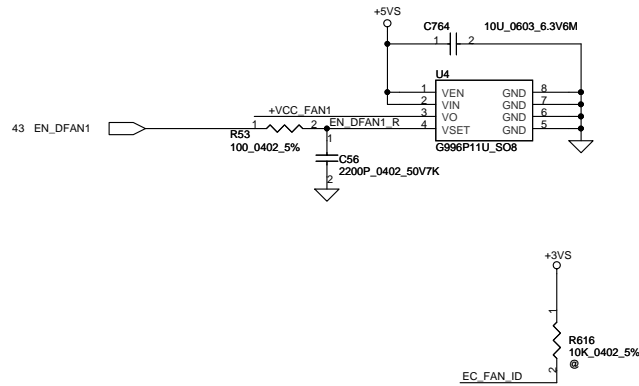


Fintek thermal sensor
placed near by TOP PCH



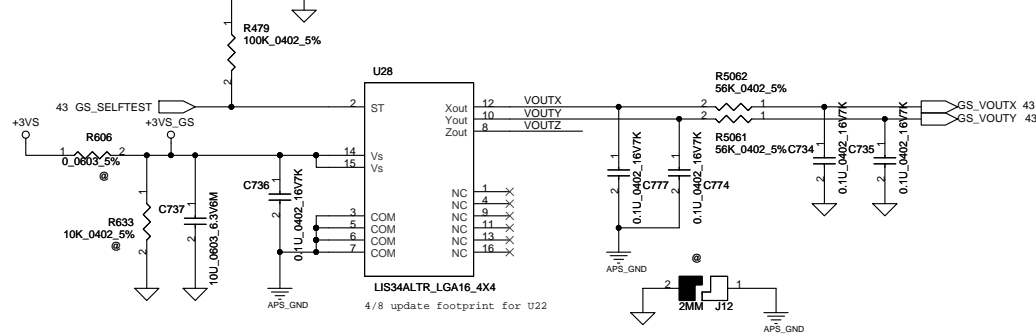
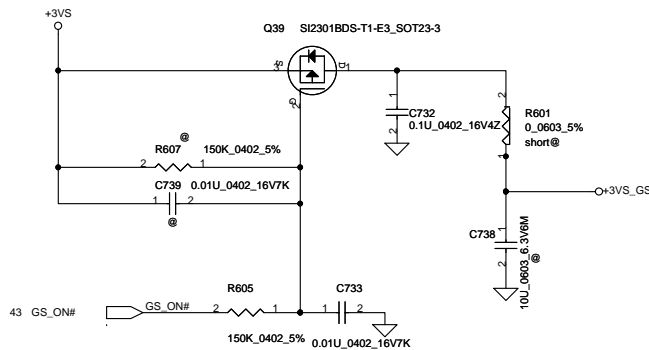
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN +5VS DROOP

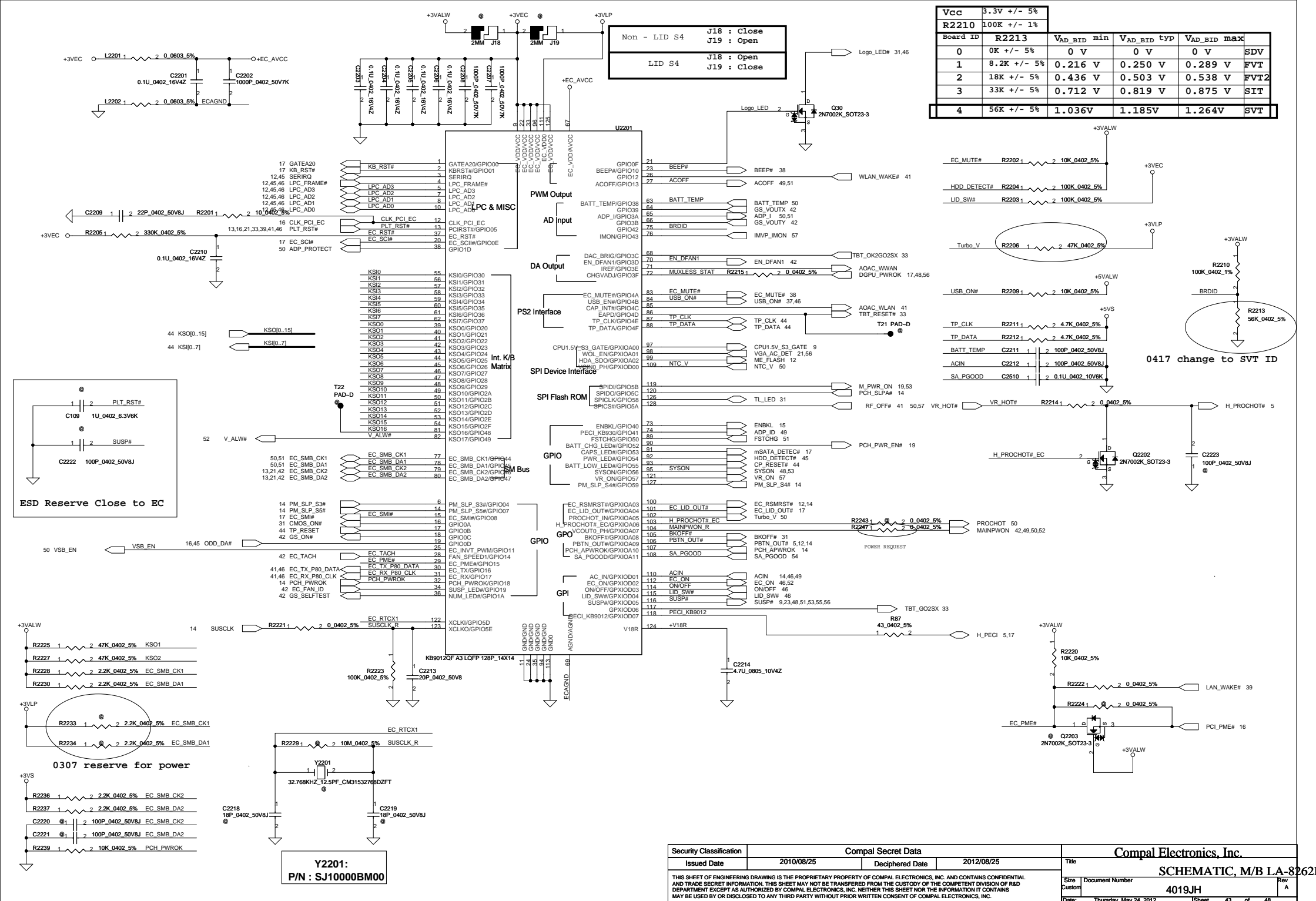


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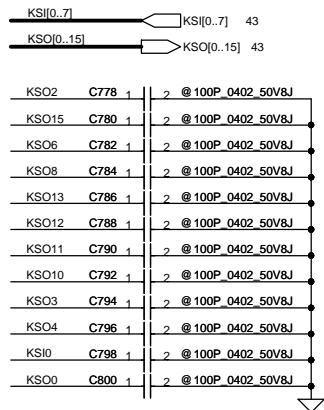
APS G-Sensor



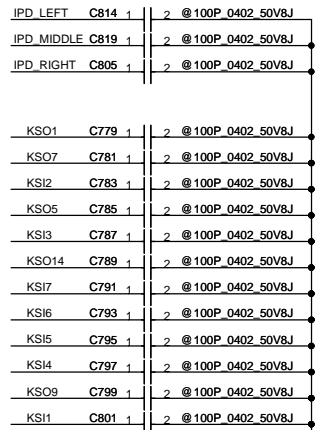
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INT_KBD Conn.



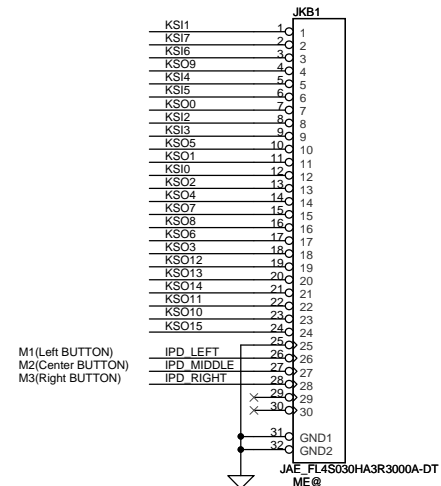
CONN PIN define need double check



Reserve for ESD.

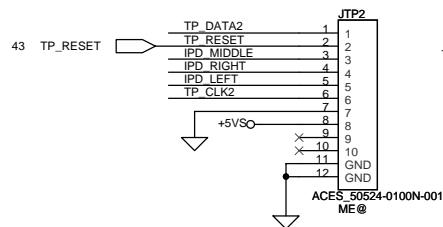
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PN:SP01000YH00



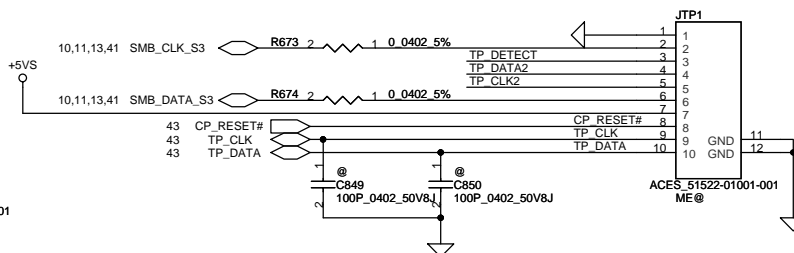
Track point

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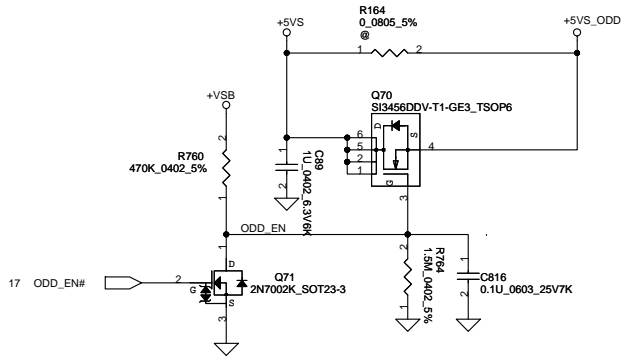
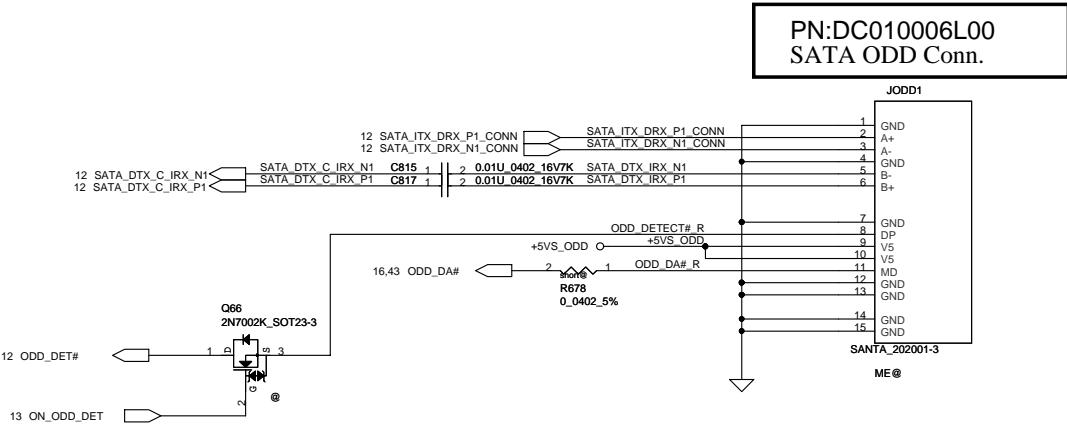
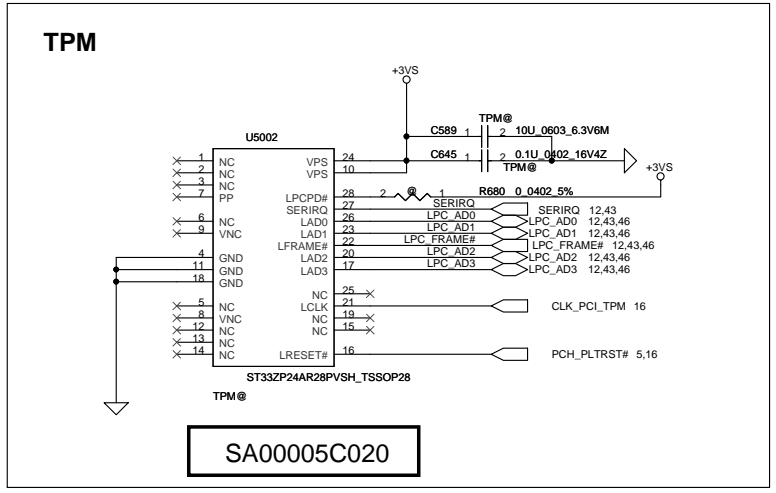
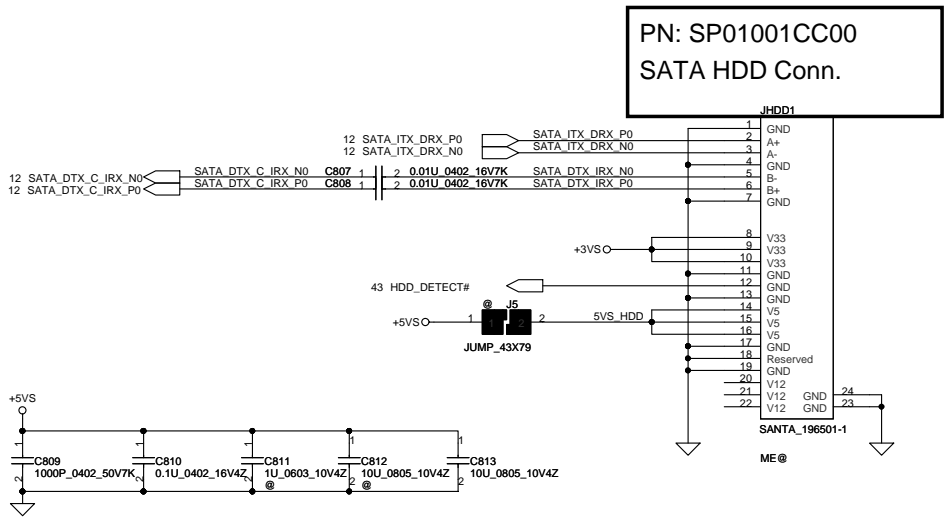
Click pad 10PIN

SP01001AL00

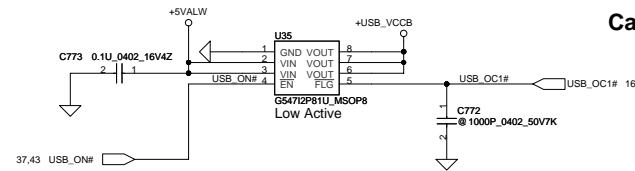
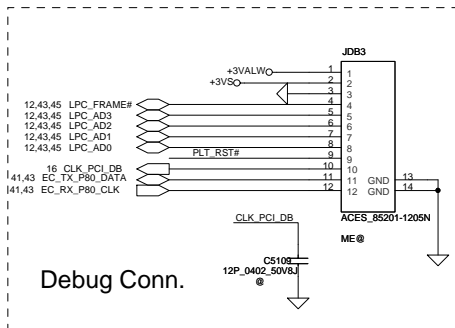
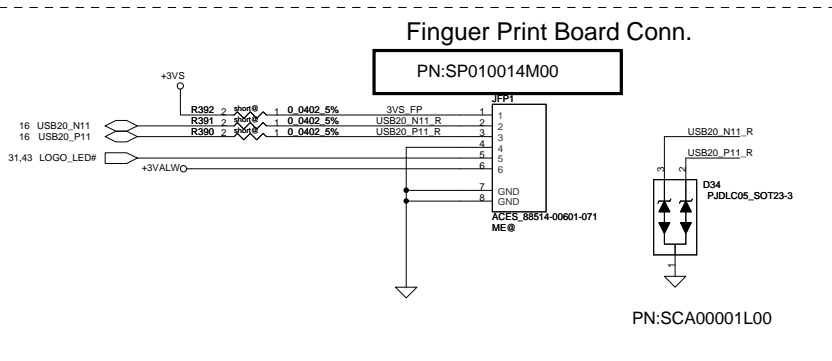
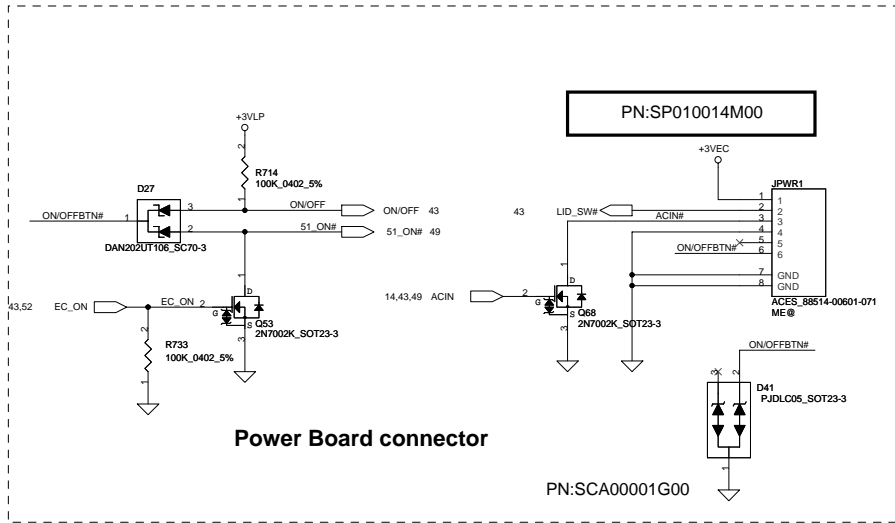


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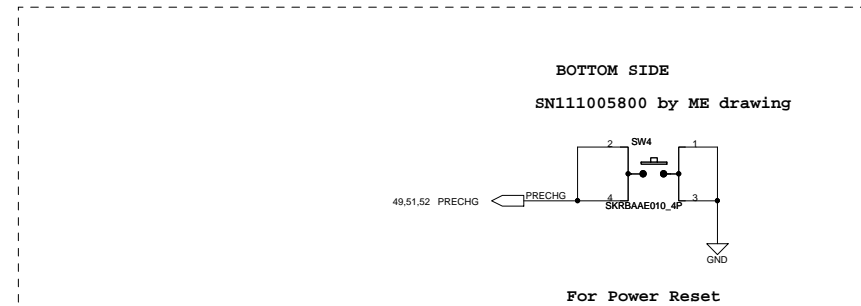
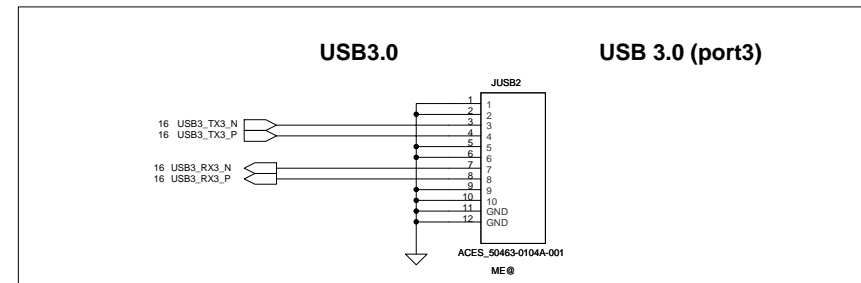
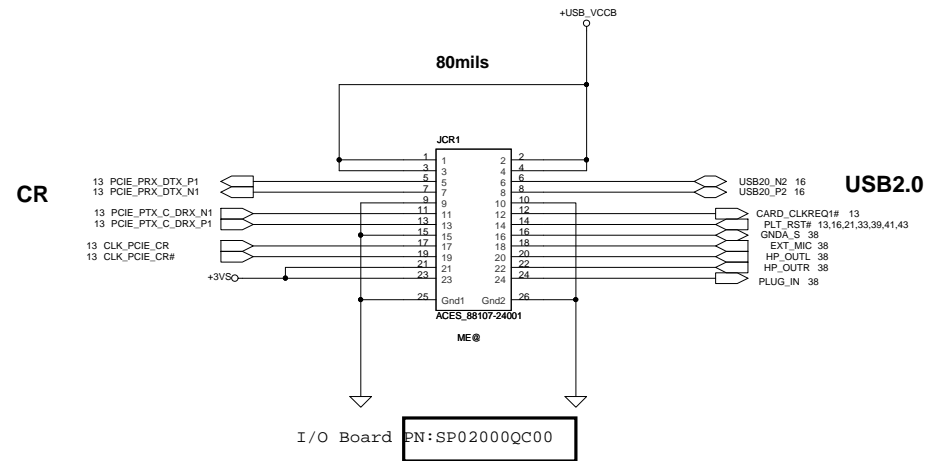
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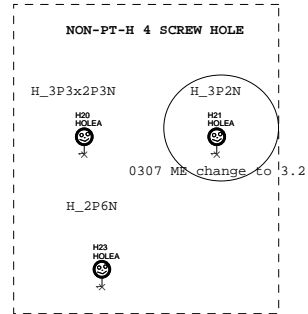
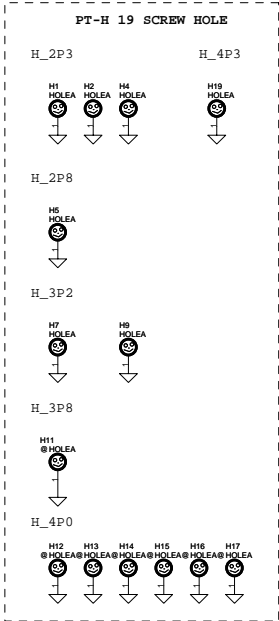
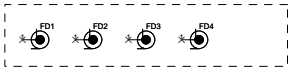
Card Reader (PCIE)

USB 2.0 (port0)

Combo Jet

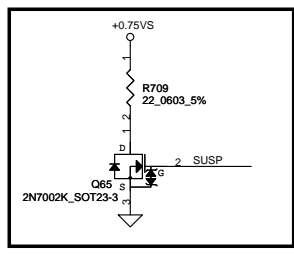
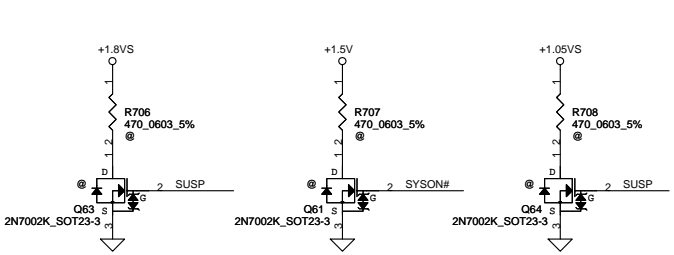
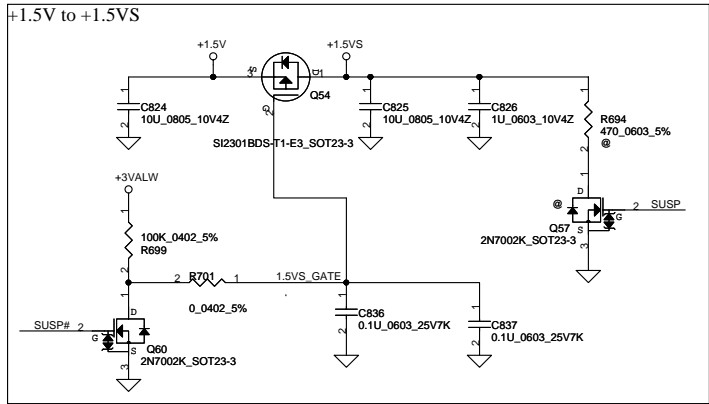
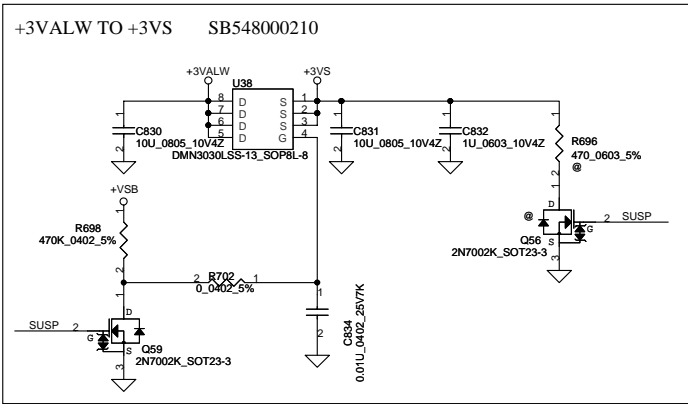
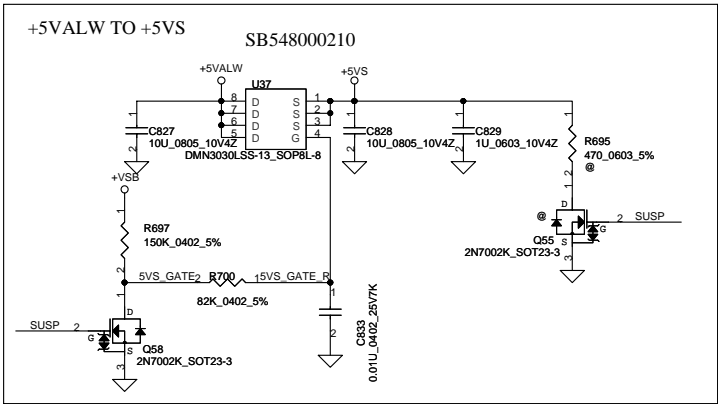


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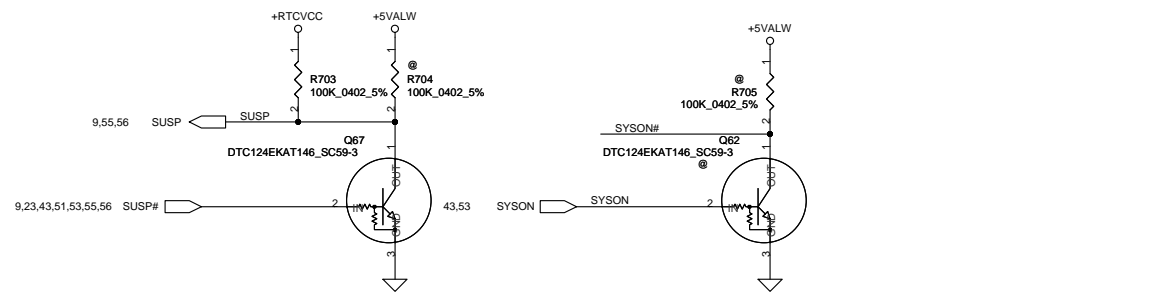


0312 Delete All sensor parts.

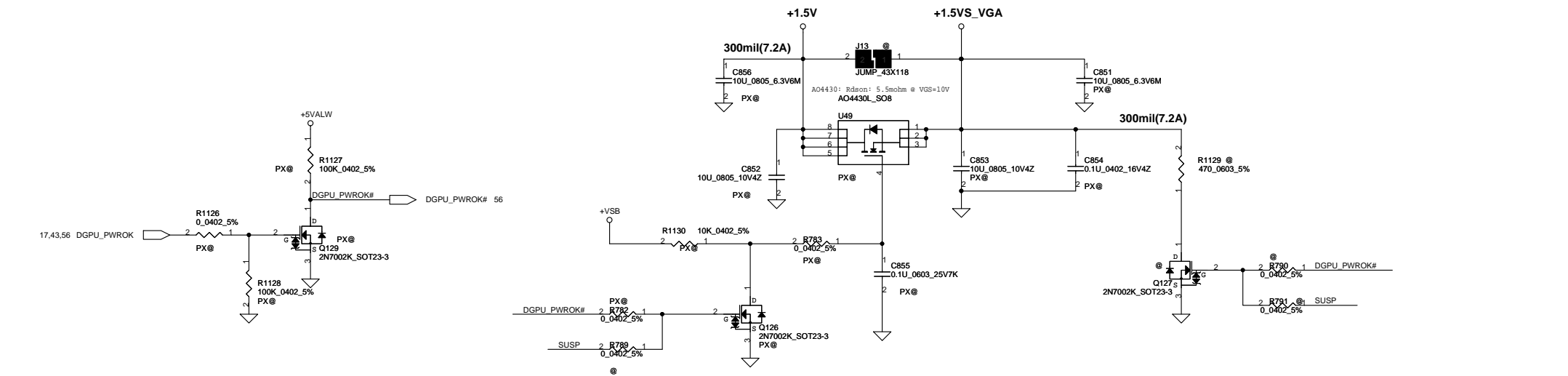
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For Intel S3 Power Reduction.



+1.5V to +1.5VS_VGA Transfer



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